

09/26/2002 09/939,457

(FILE 'HOME' ENTERED AT 11:05:54 ON 26 SEP 2002)

FILE 'INPADOC, WPIX, JAPIO, PATOSEP, PATOSWO, HCAPLUS' ENTERED AT
11:07:08 ON 26 SEP 2002

E 2000JP-255126/AP, PRN

L1

6 S E3-E4

09/26/2002 09/939,457

26sep02 11:42:17 User267149 Session D358.1

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2002/Sep W4
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File 94:JICST-EPlus 1985-2002/Jul W4
(c)2002 Japan Science and Tech Corp(JST)
*File 94: There is no data missing. UDs have been adjusted to reflect the current months data. See Help News94 for details.
File 99:Wilson Appl. Sci & Tech Abs 1983-2002/Aug
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File 108:AEROSPACE DATABASE 1962-2002/Aug
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*File 108: As of October 1, 2002,Aerospace Database will no longer be available. See HELP CSA108 for a list of alternative files.
File 144:Pascal 1973-2002/Sep W4
(c) 2002 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-2002/Sep
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*File 238: As of October 1, 2002,ANTE will no longer be available. See HELP CSA238 for a list of alternative files.
File 305:Analytical Abstracts 1980-2002/Sep W3
(c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2002/Aug
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Set	Items	Description
S1	49	AU=(IKEGAMI, G? OR IKEGAMI G?)
S2	3790	AU=(MIYOSHI, T? OR MIYOSHI T?)
S3	0	S1 AND S2
S4	0	S1 AND SEMICONDUCT?????
S5	452	S2 AND SEMICONDUCT?????
S6	0	S5 AND ((PORTABLE OR CARRY?????) (3N) (ELECTRONIC?????? OR N-OTEBOOK? ? OR NOTE()BOOK? ? OR LAPTOP? ? OR LAP()TOP ? OR VIDEO OR CAMERA? ? OR VIDEO()CAMERA))
S7	64	S5 AND (ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????)
S8	6	S7 AND ((INSULAT?????? OR DIELECTRIC???) (3N) (LAYER??? OR F-ILM??? OR COAT??? OR MULTILAYER??? OR SPACER???))
S9	5	RD (unique items)

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9/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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5192002 INSPEC Abstract Number: A9606-7360H-005, B9604-2530F-006
Title: Numerical analysis for **conduction** mechanism of thin oxide-nitride-oxide films formed on rough poly-Si
Author(s): Matsuo, N.; Fujiwara, H.; **Miyoshi, T.**; Koyanagi, T.
Author Affiliation: Dept. of Electr. & Electron. Eng., Yamaguchi Univ., Ube, Japan
Journal: IEEE Electron Device Letters vol.17, no.2 p.56-8
Publisher: IEEE,
Publication Date: Feb. 1996 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(199602)17:2L:56:NACM;1-D
Material Identity Number: I338-96002
U.S. Copyright Clearance Center Code: 0741-3106/96/\$05.00
Language: English
Abstract: The **conduction** mechanism of thin oxide-nitride-oxide films formed on rough poly-Si, in which grain sizes are not uniform, is studied for low and negative applied voltage. By assuming an electric field concentration at the convex edge of the plate **electrode**, the numerical analysis for direct tunneling (D.T.) is carried out. From the results, it is thought that the D.T. currents to the convex edge of the plate **electrode** dominate the total leakage currents.
Subfile: A B
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9/3,AB/2 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2002 Japan Science and Tech Corp(JST). All rts. reserv.

04320081 JICST ACCESSION NUMBER: 99A0730759 FILE SEGMENT: JICST-E
Analysis of Direct Thnneling for Thi SiO2 Film.
MATSUO N (1); MIURA T (1); URAKAMI A (1); **MIYOSHI T** (1)
(1) Yamaguchi Univ., Ube, Jpn
Jpn J Appl Phys Part 1, 1999, VOL.38,NO.7A, PAGE.3967-3971, FIG.8, REF.5
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382 MIS
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The direct tunneling (DT) currents of the metal insulator metal (MIM) structure is presented theoretically by considering the relationship between the applied voltage to the oxide film (oxide voltage: VOX) and the Fermi energy (.ETA.) of the metal. Using the newly obtained equation, the DT of a poly-Si/SiO2/p-Si(100) stacked structure is analyzed. For eVOX<.ETA., the current component relating to the Fermi energy of the **electrode** is added to Simmons' equation. The dependence of each term for the present function, which is composed of the DT current flowing from the high-potential

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electrode to the low-potential one, reverse DT currents and the current component relating to the Fermi energy on the oxide voltage was examined. For **eVOX>.ETA.**, a new formula is introduced, since the DT currents are not calculated by Simmons' equation theoretically. The present calculation reproduces the large increase in ratio of the currents for **eVOX<.ETA.**, and the accurate absolute value of the currents for **eVOX>.ETA.** The reason why the calculated results are still large, one order of magnitude at the maximum, as compared with the measured data from 0 to approximately -0.5 V is also discussed from the viewpoints of the multifold valleys of Si, inelastic scattering and Fermi distribution. (author abst.)

9/3,AB/3 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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03704408 JICST ACCESSION NUMBER: 98A0800779 FILE SEGMENT: JICST-E
Theoretical Study of Si Resonant Tunneling MOS Transistor.
MATSUO N (1); MIURA T (1); HAMADA H (1); NAKATA S (1); **MIYOSHI T** (1)
(1) Yamaguchi Univ., Ube, Jpn
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report
(Institute of Electronics, Information and Communication Enginners),
1998, VOL.98,NO.195(ICD98 75-90), PAGE.25-30, FIG.7, REF.10

JOURNAL NUMBER: S0532BBG

UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: New MOST(metal oxide **semiconductor** transistor) with the thin **dielectric film** at the both edges of the channel (Si Resonant Tunneling MOST: SIRTMOST) is investigated. The potential and the electric field of the channel, the transconductance g_m and the subthreshold swing S-value of the SIRTMOST are calculated. Assuming the asymmetric SiO₂ at the both edges of the channel, g_m and S-value of the SIRTMOST are compared with those of the conventional(Conv.) MOST. It is also shown that the double-barriers formed at the both edges of the channel extends the physical limit of the Conv. MOST. (author abst.)

9/3,AB/4 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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03134309 JICST ACCESSION NUMBER: 97A0205947 FILE SEGMENT: JICST-E
Theoretical Analysis for **Conduction** Mechanism of Thin
Oxide-Nitride-Oxide Films in the Range of Low Voltage by WKB
Approximation.

MATSUO NAOTO (1); FUJIWARA HIROAKI (1); **MIYOSHI TADAKI** (1)

(1) Yamaguchi Univ., Fac. of Eng.

Denshi Joho Tsushin Gakkai Ronbunshi. C,2(Transactions of the Institute of
Electronics, Information and Communication Engineers. C-2), 1997,
VOL.80,NO.1, PAGE.23-30, FIG.7, REF.20

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JOURNAL NUMBER: L0196AAD ISSN NO: 0915-1907
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

ABSTRACT: In a ruggedness polycrystal Si storage **electrode** which has an uneven crystal grain size, and an oxidation and nitriding and oxidation composite membrane, and the leakage current and the applied voltage characteristics of a capacitor which is consisted of an polycrystal Si plate **electrode**, the leakage current which is compared with a plate type STC is increased more than a capacity area ratio, when a negative voltage is applied to a plate **electrode**. In a plate **electrode** edge part which is formed in adjoining grains, an electric field concentration is occurred, and by assuming that it is directly induced tunneling, this phenomenon is theoretically analyzed by a WKB approximation. In addition, the radius of curvature of a plate **electrode** edge which is assumed as a part of a ball is calculated the leakage current, on the assumption that it is regularly distributed in an one capacitor array. By the standard deviation in the normal distribution of an electric field concentration factor, effective mass and a plate **electrode** edge part radius of curvature, the fitting for applied voltage characteristics and a leakage current which is measured is made, and its result is discussed. On the assumption that the electric field concentration factor is 1.5, the effective mass is $0.25m_0$ (m_0 is the mass in the electronic vacuum) and the standard deviation is 1.5nm, the increasing rate of a leakage current which is obtained by a calculation is in an extent that the applied voltage is from -2.5V to -3.0V, and it is shown an approximation, though it is not exactly in accordance with the measured value. Then, the phenomenon in which a capacitor leakage current with ruggedness polycrystal Si is increased more than a capacity area ratio with STC can be explained. Some considerations on the reasons for which the increasing rate to an applied voltage of a leakage current which is obtained by the calculation is not accorded with the measured value is made.

9/3,AB/5 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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01908330 JICST ACCESSION NUMBER: 93A0721213 FILE SEGMENT: JICST-E
Special issue : Liquid crystal projector of which advance is remarkable.
ILA (image light amplifier) super projector.

MIYOSHI TADAYOSHI (1)
(1) Victor Co. of Japan, Ltd.
O plus E, 1993, NO.165, PAGE.71-76, FIG.6, TBL.1, REF.4
JOURNAL NUMBER: Z0994AAN ISSN NO: 0911-5943
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Review article
MEDIA TYPE: Printed Publication

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26sep02 12:03:21 User267149 Session D359.1

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2002/Sep W4
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*File 34: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
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*File 77: As of October 1, 2002,Conference Papers Index will no longer be available. See HELP CSA77 for a list of alternative files.
File 94:JICST-EPlus 1985-2002/Jul W4
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*File 94: There is no data missing. UDs have been adjusted to reflect the current months data. See Help News94 for details.
File 99:Wilson Appl. Sci & Tech Abs 1983-2002/Aug
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File 108:AEROSPACE DATABASE 1962-2002/Aug
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*File 108: As of October 1, 2002,Aerospace Database will no longer be available. See HELP CSA108 for a list of alternative files.
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*File 238: As of October 1, 2002,ANTE will no longer be available. See HELP CSA238 for a list of alternative files.
File 305:Analytical Abstracts 1980-2002/Sep W3
(c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2002/Aug
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File 350:Derwent WPIX 1963-2002/UD,UM &UP=200261
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*File 350: Alerts can now have images sent via all delivery methods.

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See HELP ALERT and HELP PRINT for more info.

File 347:JAPIO Oct 1976-2002/May(Updated 020903)

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*File 347: JAPIO data problems with year 2000 records are now fixed.

Alerts have been run. See HELP NEWS 347 for details.

File 344:Chinese Patents Abs Aug 1985-2002/Sep

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File 371:French Patents 1961-2002/BOPI 200209

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*File 371: This file is not currently updating. The last update is 200209.

09/26/2002 09/939,457

Set	Items	Description
S1	1160267	(PORTABLE OR CARRY?????)
S2	22556	(PORTABLE OR CARRY?????) (3N) (ELECTRONIC?????? OR NOTEBOOK? ? OR NOTE()BOOK? ? OR LAPTOP? ? OR LAP()TOP ? OR VIDEO OR CAM- ERA? ? OR VIDEO()CAMERA)
S3	16132	(PORTABLE OR CARRY?????) (3N) APPARAT??????
S4	16132	(PORTABLE OR CARRY?????) (3N) APPARAT??????
S5	201571	(SMALL?????? OR MINIM?????? OR REDUC??????) (3N) (DIMENSION? ? OR WEIGHT???)
S6	243110	(REDUCT?????? OR LOWER???? OR MINIM??????) (3N) COST?????
S7	1583818	S1:S6
S8	2444969	SEMICONDUCT?????
S9	7290	CC=B2560 Semiconductor devices
S10	5072	MC=S01-G02B
S11	99931	IC=G01R-031
S12	2523113	S8:S11
S13	60511	SEMICONDUCT?????? (3N) CHIP? ?
S14	623	SANDWICH?????? (3N) CIRCUIT???
S15	61125	S13:S14
S16	4121293	ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????
S17	409774	(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????) (3N) (LAY- ER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S18	12099	CC=(B2110 OR B2160 OR B8130)
S19	4759	MC=(S05-A02 OR S05-D01A1A OR U11-C05C4)
S20	7770	IC=(A61N-001/04 OR A61N-001/06 OR A61B-005/04)
S21	4779	MC=(V05-D07C5C OR V07-F01A1)
S22	108815	IC=(H01J-029/89 OR G02B-006)
S23	4234668	S16:S22
S24	17678	(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????) (3N) (REAR OR BACK)
S25	4074	PROTRUD?????? (3N) (ELECTRODE? ? OR MICROELECTRODE? ? OR CON- DUCT?????)
S26	7318	(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????) (3N) FRONT
S27	8708	BUMP?????? (3N) (ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT- T?????)
S28	19865	S25:S27
S29	418475	*deleted* (INSULAT?????? OR DIELECTRIC???) (3N) (LAYER??? OR FILM??? OR COAT??? S OR MULTILAYER??? OR SPACER???)
S30	12886	MC=(U11-C06A1B OR U11-C07C3 OR U11-C08A1 OR U11-C08A6)
S31	27957	CC=(A5150 OR A7700 OR B2800 OR B2810 OR B2830)
S32	443153	(INSULAT?????? OR DIELECTRIC???) (3N) (LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S33	475639	S30:S32
S34	241309	RESIN??? (N3) (LAYER????? OR FILM??? OR COAT???)
S35	517117	(EPOX??? OR RESIN? ? OR THERMOPLASTIC??? OR ELASTOMER?? OR RUBBER? ? OR ADHESIVE??) (N3) (LAYER??? OR FILM??? OR COAT???)
S36	3248856	POLYMER????
S37	9627	MC=U11-E02A1
S38	18589	IC=H01L-021/56
S39	3578959	S34:S38
S40	174394	(INTERCONNECT?????? OR CONNECT??????) (3N) (LINE? ? OR LININ- G)
S41	4424578	(INTERCONNECT?????? OR CONNECT??????)

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S42	4424578	S40:S41
S43	172634	PRINT?????(3N)CIRCUIT??????
S44	181224	CIRCUIT?????(3N)BOARD??????
S45	245594	S43:S44
S46	43523	(WIRE?? OR WIRING) (3N)BOND??????
S47	52615	S7 AND S12
S48	4001	S47 AND S15
S49	1402	S48 AND S23
S50	175	S49 AND S28
S51	19	S50 AND S33
S52	19	RD (unique items)
S53	156	S50 NOT S52
S54	34	S53 AND S39
S55	25	S54 AND S42
S56	7	S55 AND S45
S57	7	RD (unique items)
S58	18	S55 NOT S57
S59	18	RD (unique items)
S60	9	S54 NOT S55
S61	9	RD (unique items)
S62	122	S53 NOT S54
S63	0	S62 AND S34
S64	101	S62 AND S1
S65	3	S64 AND S5
S66	98	S64 NOT S65
S67	0	S66 AND S14
S68	0	S66 AND S32
S69	2	S66 AND S6
S70	96	S66 NOT S69
S71	4	S70 AND S25
S72	4	RD (unique items)
S73	92	S70 NOT S72
S74	8	S73 AND S24
S75	8	RD (unique items)

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52/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014284629

WPI Acc No: 2002-105330/200214
Related WPI Acc No: 2001-440619
XRAM Acc No: C02-032305
XRPX Acc No: N02-078320

Interconnection of electronic components utilizes **conductive** studs of first electronic component e.g., **semiconductor chip**, and corresponding **conductive** vias of second electronic component e.g., chip carrier

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: BROFMAN P J; RAY S K; STALTER K A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010019178	A1	20010906	US 99315374	A	19990518	200214 B
			US 2001825512	A	20010403	

Priority Applications (No Type Date): US 99315374 A 19990518; US 2001825512 A 20010403

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010019178	A1		7	H01L-029/40	Div ex application US 99315374 Div ex patent US 6258625

Abstract (Basic): US 20010019178 A1

Abstract (Basic):

NOVELTY - Electronic components are interconnected by utilizing **conductive** studs on a surface of a first electronic component, and corresponding **conductive** vias on a surface of a second electronic component. The studs and the vias are adapted to be electrically interconnected by an interposer disposed between the first and second electronic components.

DETAILED DESCRIPTION - Interconnection of electronic components involves providing a first electronic component (12) having electrical devices with corresponding bonding pads. The first electronic component includes a patterned **dielectric film** (30A) having **protruding conductive** studs (40A). The studs correspond to the bonding pads and are adapted for electrical connection to the electrical devices. A second electronic component (15), which includes a **dielectric film** (50) having **conductive** vias (60), is provided. The **conductive** vias correspond to the studs on the first electronic component. An interposer (100), which has electrical interconnections corresponding to the studs and vias, is provided. The first and second electronic components are then aligned with the interposer disposed between them. The studs of the first electronic component and the vias of the second electronic component are adapted to be electrically interconnected by the interposer.

An INDEPENDENT CLAIM is also included for an electronic module comprising the first and second electronic components, and the

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interposer disposed between the electronic components.

USE - For interconnecting electronic components, e.g. **semiconductor chip** and **chip** carrier.

ADVANTAGE - The inventive method utilizes lead-free interconnects which do not require flux and takes into account the deformities on a substrate surface.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view illustrating the interconnection of a chip and a chip carrier with an interposer.

First electronic component or **semiconductor chip** (12)

Second electronic component or chip carrier (15)

Dielectric films (30A, 50)

Conductive vias (60)

Interposer (100)

Conductive metal vias (150)

pp; 7 DwgNo 4/5

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52/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014029411

WPI Acc No: 2001-513625/200156

XRAM Acc No: C01-153463

XRPX Acc No: N01-380424

Semiconductor device e.g. flip-chip ball grid array packaged device
has **insulating** resin **layer** covering projecting
electrode, post **electrode** and passivation **film**, except
end face of post **electrode**

Patent Assignee: NEC CORP (NIDE)

Inventor: MIYAZAKI T

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010010945	A1	20010802	US 2001770458	A	20010129	200156 B
JP 2001217340	A	20010810	JP 200024094	A	20000201	200160
KR 2001078174	A	20010820	KR 20014451	A	20010131	200212

Priority Applications (No Type Date): JP 200024094 A 20000201

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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US 20010010945	A1		15	H01L-021/44	
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JP 2001217340	A		11	H01L-023/12	
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KR 2001078174	A			H01L-023/52	
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Abstract (Basic): US 20010010945 A1

Abstract (Basic):

NOVELTY - Metal **bumps** are provided on **electrode** pads
formed on **semiconductor chip**. A passivation film formed on
the chip has openings for exposing the pads. A projecting
electrode is connected to the pads and the post **electrode**
connects the other end of the projecting **electrode** with the
bumps. An **insulating** resin **layer** covers the two
electrodes and the passivation **film**, except end face of the
post **electrode**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for
semiconductor device manufacturing method.

USE - E.g. flip chip ball grid array (FCBGA) type packaged device
in large scale **semiconductor** device (LSI) used in **portable**
electronic equipment.

ADVANTAGE - The heat and mechanical stress on the passivation film
metal bump is moderated by the **insulating** resin **layer**, and
a multilayered wiring board with reduced cost and size is obtained.

DESCRIPTION OF DRAWING(S) - The figure shows the two metal layer on
the clad metal plate used for manufacturing flip **chip** type
semiconductor device.

pp; 15 DwgNo 1A/10

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52/3,AB/3 (Item 3 from file: 350)
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013963779

WPI Acc No: 2001-447993/200148

XRPX Acc No: N01-331638

Bilayered circuit tape carrier for mounting **semiconductor chip** on circuit board, has columnar metal **bump** formed over **conductor** pattern formed on **insulated film**

Patent Assignee: FURUKAWA ELECTRIC CO LTD (FURU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001156121	A	20010608	JP 99336137	A	19991126	200148 B

Priority Applications (No Type Date): JP 99336137 A 19991126

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001156121	A	19	H01L-021/60	

Abstract (Basic): JP 2001156121 A

Abstract (Basic):

NOVELTY - **Conductor** (16) is provided in through-hole formed in **insulated film** (11). A **conductor** pattern (15) is formed on one main surface of **insulated film** and joined to **conductor**. Another **conductor** pattern (12) is formed in other main surface. Columnar metal bump (13) having vertical side perpendicular to **conductor** face, is formed on **conductor** pattern (12).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of tape carrier.

USE - For mounting **semiconductor chip** on circuit board.

ADVANTAGE - Since metal bump has columnar shape, pitch between bumps can be made smaller, and formation of bridge between bumps is prevented.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of bilayered circuit tape carrier.

Insulated film (11)

Conductor patterns (12,15)

Metal bump (13)

Conductor (16)

pp; 19 DwgNo 1/23

09/26/2002 09/939,457

52/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013669934

WPI Acc No: 2001-154146/200116

XRFX Acc No: N01-113718

Semiconductor device mounting structure for **portable**
electronic device, has diffusion junction containing mixture of
metals and anisotropic electroconductive resin for connecting
electrode pad with circuit **electrode**

Patent Assignee: CITIZEN WATCH CO LTD (CITL)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000357710	A	20001226	JP 2000109040	A	20000411	200116 B

Priority Applications (No Type Date): JP 99109201 A 19990416

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000357710	A	11	H01L-021/60	

Abstract (Basic): JP 2000357710 A

Abstract (Basic):

NOVELTY - **Electrode** pad (14) provided in the hole (16a) of
insulating film (16) of **semiconductor** device (10),
contacts circuit **electrode** (28) provided on circuit board (26),
through a diffusion junction. Anisotropic electroconductive resin (20)
mixed with metals like gold or platinum (18) is interposed between
electrode pad and circuit **electrode**, forming diffusion
junction.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for
mounting procedure of **semiconductor** device.

USE - For mounting **semiconductor** device such as integrated
circuit, large scale integrated circuit (LSIC) for **portable**
electronic devices and liquid crystal display device.

ADVANTAGE - Since **semiconductor** device and circuit board are
connected by diffusion junction containing mixture of metals and
anisotropic electroconductive resin, the connections are reliable and
high density mounting is realized. Since **bump electrode** is
not formed on **semiconductor** device for connection purposes,
manufacturing steps are reduced due to which cost is reduced. Avoids
crack generation in protective coat of **semiconductor chip**,
thereby reliable mounting structure is achieved.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of
mounting structure of **semiconductor** device.

Semiconductor device (10)

Electrode pad (14)

Insulating film (16)

Hole (16a)

Platinum (18)

Anisotropic electroconductive resin (20)

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/26/2002 09/939,457

52/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013560995

WPI Acc No: 2001-045202/200106

XRPX Acc No: N01-034307

Micro ball grid array type **semiconductor** device, includes openings formed on **insulating layers** so as to expose **conductive layer** to **front** and rear surface of chip

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)

Inventor: KOMIYAMA M

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000307029	A	20001102	JP 99117442	A	19990426	200106 B
US 6329708	B1	20011211	US 2000536763	A	20000328	200204

Priority Applications (No Type Date): JP 99117442 A 19990426

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000307029	A		11	H01L-023/12	
US 6329708	B1			H01L-023/48	

Abstract (Basic): JP 2000307029 A

Abstract (Basic):

NOVELTY - Integrated circuit with external terminal (104) is formed on front of **semiconductor chip** (101). A **conductive layer** (110) of tape (108) electrically connected with external terminal (104) is formed extending from front to rear sides of chip.

Layer (110) is formed between **insulating layers** (109,113).

Openings (103a,103b) formed on **insulating layers** expose

conductive layers to **front** and rear sides of chip.

DETAILED DESCRIPTION - The tape (108) comprising **multilayered** structure of **conductive** and **insulating layers**

(109,110,113) is fixed with the **semiconductor chip** through

a buffer **film**. The connection of **conductive layer** and

the external terminal is covered by resin. An INDEPENDENT CLAIM is also included for **semiconductor** module.

USE - Micro ball grid array type **semiconductor** device.

ADVANTAGE - Since **conductive layer** is exposed to chip surface from openings, on **insulating layer** and is electrically connected with external device, mounting of **semiconductor** device is simplified, thus achieving **cost reduction**.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of structure of **semiconductor** device.

Semiconductor chip (101)

Opening (103a,103b)

External terminal (104)

Tape (108)

Insulating layers (109,113)

Conductive layer (110)

09/26/2002 09/939,457

52/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013523977

WPI Acc No: 2001-008183/200102

XRPX Acc No: N01-005982

Band carrier for ball grid array (BGA) used with **semiconductor**
flip-**chip** with pads in linear arrangement

Patent Assignee: HITACHI CABLE LTD (HITD)

Inventor: HOSONO M; KAMEYAMA Y; OKABE N

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 10002426	A1	20000727	DE 1002426	A	20000120	200102 B
JP 2000216202	A	20000804	JP 9912956	A	19990121	200102
JP 2000243863	A	20000908	JP 9939406	A	19990218	200102
KR 2000053570	A	20000825	KR 20002843	A	20000121	200121
TW 448548	A	20010801	TW 2000100924	A	20000120	200222
US 6376916	B1	20020423	US 2000488507	A	20000120	200232

Priority Applications (No Type Date): JP 9939406 A 19990218; JP 9912956 A
19990121

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10002426	A1		22	H01L-023/50	
JP 2000216202	A		6	H01L-021/60	
JP 2000243863	A		6	H01L-023/12	
KR 2000053570	A			H01L-023/28	
TW 448548	A			H01L-023/12	
US 6376916	B1			H01L-029/40	

Abstract (Basic): DE 10002426 A1

Abstract (Basic):

NOVELTY - The BGA band carrier comprises an **insulating film** with an aperture in its middle and numerous **conductors** on it, **protruding** into the aperture to form numerous inner **conductors**, to which are coupled numerous protrusions, both **conductors** and protrusions arranged in a preset pattern. There is an elastomer layer, relieving thermal load, located on a surface of the **insulating film** by an adhesive such that they are located on opposite side of the aperture, separated round one or two ends of the aperture, the layers are of adhesive film of resin with low elasticity.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for a **semiconductor** component.

USE - For **semiconductor** component with flip-**chip**.

ADVANTAGE - No cavities in sealing resin and reduced thermal load.

DESCRIPTION OF DRAWING(S) - The figure shows a plan view of band carrier according to invention.

pp; 22 DwgNo 8/18

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/26/2002 09/939,457

52/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013058055

WPI Acc No: 2000-229923/200020

Related WPI Acc No: 2000-212135

XRPX Acc No: N00-173130

Tape carrier structure for **semiconductor** device package, includes
columnar bump section projecting vertically from copper patterns formed
on the **insulating film**

Patent Assignee: FURUKAWA ELECTRIC CO LTD (FURU)

Inventor: AMANO T; ASADA T; HAMADA M

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000049197	A	20000218	JP 99112254	A	19990420	200020 B
US 6100112	A	20000808	US 98167012	A	19981006	200040
TW 440973	A	20010616	TW 98116623	A	19981007	200203

Priority Applications (No Type Date): JP 98147753 A 19980528; JP 98147754 A
19980528

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000049197	A		11	H01L-021/60	
US 6100112	A			H01L-021/44	
TW 440973	A			H01L-021/60	

Abstract (Basic): JP 2000049197 A

NOVELTY - Copper patterns (12) are formed on the **insulating film** (11) of the circuit board. Metallic bumps (13) comprising columnar section projecting vertically to the pattern is formed on the patterns. The **semiconductor chip** is connected with the bumps. DETAILED DESCRIPTION - A hole is formed on the lower side of insulating flame for extracting connection terminal. The junction **electrode** (14) is formed on the hole. Both pattern and circuit board are connected to the **electrode**. An INDEPENDENT CLAIM is also included for tape carrier manufacturing method.

USE - For tape carrier used in **semiconductor** device package.

ADVANTAGE - Reduces size of package by projecting bump vertically from the pattern. Improves mechanical strength by using metal bumps.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of tape carrier. (11) **Insulating film**; (12) Copper patterns; (13)

Metallic **bumps**; (14) Junction **electrode**.

Dwg.1/13

09/26/2002 09/939,457

52/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013040282

WPI Acc No: 2000-212135/200019

Related WPI Acc No: 2000-229923

XRFX Acc No: N00-158931

Semiconductor chip mounting method for **semiconductor** device manufacture, involves fixing **semiconductor chip** on tape carrier and connecting **electrodes** of **semiconductor chip** to metal **bumps** formed on **conductor** pattern

Patent Assignee: FURUKAWA ELECTRIC CO LTD (FURU)

Inventor: AMANO T; ASADA T; HAMADA M

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11340276	A	19991210	JP 98147754	A	19980528	200019 B
US 6100112	A	20000808	US 98167012	A	19981006	200040
TW 440973	A	20010616	TW 98116623	A	19981007	200203

Priority Applications (No Type Date): JP 98147754 A 19980528; JP 98147753 A 19980528

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11340276	A		7	H01L-021/60	
US 6100112	A			H01L-021/44	
TW 440973	A			H01L-021/60	

Abstract (Basic): JP 11340276 A

NOVELTY - **Conductor** pattern (12) is formed on the **insulated film** (11), over which metallic **bumps** (13) are formed. **Electrodes** (22) of the **semiconductor chip** are located on the metal bump and the chip is fixed on the **insulating film** by the thermosetting resin (25). The metal bump are made to melt by heating and **electrode** of the chip are connected to the metal bumps.

USE - For **semiconductor** device manufacture.

ADVANTAGE - Bump height is lowered, thus position gap of **semiconductor chip** is avoided. By melting metal **bumps**, **electrodes** of **semiconductor** are connected to metal bumps reliably. DESCRIPTION OF DRAWING(S) - The figure shows sectional view explaining manufacture process of **semiconductor** package. (11) **Insulated film**; (12) **Conductor** pattern; (13) Metal **bumps**; (22) **Electrodes**; (25) Thermosetting resin.

Dwg.2/5

09/26/2002 09/939,457

52/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012770620

WPI Acc No: 1999-576843/199949

XRAM Acc No: C99-168086

XRPX Acc No: N99-426002

Heat surface type magnetic inductor for micro-electric power converter

e.g. DC-DC converter, transformer - provides **bump electrode**

functioning as terminal of coil **conductor**

Patent Assignee: FUJI ELECTRIC CO LTD (FJIE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11251157	A	19990917	JP 98354467	A	19981214	199949 B

Priority Applications (No Type Date): JP 97345158 A 19971215

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11251157	A		8	H01F-027/28	

Abstract (Basic): JP 11251157 A

NOVELTY - A coil **conductor** (27) is pinched inbetween a pair of magnetic thin films (24a, 24b) on a silicon wafer (21) via **insulating films** (23a, 23b). A **bump electrode** is provided on the terminal of the coil **conductor**.

USE - For DC-DC convertor, transformer used for **portable electronic information apparatus**.

ADVANTAGE - Mounting procedure of the **semiconductor chip** is improved and size is reduced as the inductor is formed with flat surface.

DESCRIPTION OF DRAWING(S) - The figure shows the fragmentary sectional view of micro-electric power convertor and sectional view of flat surface type coil. (21) Silicon wafer; (23a,23b) **Insulating films**; (24a,24b) Magnetic thin **films**; (27) Coil **conductor**.

Dwg.1/9

09/26/2002 09/939,457

52/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012698394

WPI Acc No: 1999-504503/199942

XRPX Acc No: N99-377311

External connection **electrode** formation method in tape carrier type
semiconductor package - involves connecting external
electrodes to **semiconductor chip**, projecting out of
flat surface of **semiconductor** package

Patent Assignee: HITACHI LTD (HITA); HITACHI MICON SYSTEM KK (HITA-N)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11220058	A	19990810	JP 9822861	A	19980204	199942 B

Priority Applications (No Type Date): JP 9822861 A 19980204

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11220058	A	10	H01L-023/12	

Abstract (Basic): JP 11220058 A

NOVELTY - **Semiconductor chip** (2) is sealed in a sealing
body (7). **Electrodes** (4) for external connection supported on
insulating films (5A,5B) and connected to
semiconductor through **bump electrode** (6), projects
out of sealing body all along the flat surface.

USE - In tape carrier type **semiconductor** package.

ADVANTAGE - As external leads are brought out all along the package
surface, surface size is reduced for given number of connections.

Reliability of connection between **semiconductor** device and
substrate is enhanced. DESCRIPTION OF DRAWING(S) - The diagram shows
sectional view of **semiconductor** device. (2) **Semiconductor**

chip; (4) **Electrodes**; (5A,5B) **Insulating films**;

(6) **Bump electrode**; (7) Sealing body.

Dwg.2/15

09/26/2002 09/939,457

52/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012353360

WPI Acc No: 1999-159467/199914

XRPX Acc No: N99-116064

Semiconductor package manufacturing method - involves performing thermocompression breadth side bonding of **semiconductor chip** and carrier film by pressing chip and carrier film after supply of liquid state resin binder between them

Patent Assignee: SUMITOMO METAL MINING CO (SUMM)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11016941	A	19990122	JP 97163601	A	19970620	199914 B

Priority Applications (No Type Date): JP 97163601 A 19970620

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11016941	A	6	H01L-021/60	

Abstract (Basic): JP 11016941 A

NOVELTY - A **bump electrode** formed on an **electrode** pad of a **semiconductor chip** (1) is connected electrically to a carrier film. **Insulated** liquid state resin binder (2) is supplied between the **semiconductor chip** and the carrier film after which the **semiconductor chip** is pressed against the carrier film by a presser (7) thereby performing thermocompression bonding and breadthwise sealing of **semiconductor chip** to the carrier film.

USE - The **semiconductor** package is used for various electronic machines.

ADVANTAGE - Enables to obtain a reliable **semiconductor** package. The amount of binder used is economized. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of **semiconductor** package. (1) **Semiconductor chip**; (2) Binder; (7) Presser.

Dwg.1/4

09/26/2002 09/939,457

52/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011539092

WPI Acc No: 1997-515573/199748

XRFX Acc No: N97-428884

Tape carrier package for connecting circuits to LCD device - has tape carrier with **conductive** pattern that has leads protruding through holes connecting chips and anisotropic cover

Patent Assignee: SHARP KK (SHAF)

Inventor: TAJIMA N

Number of Countries: 007 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 803906	A2	19971029	EP 97302841	A	19970425	199748 B
JP 9292624	A	19971111	JP 96108288	A	19960426	199804
KR 97072373	A	19971107	KR 9715782	A	19970426	199846
TW 375694	A	19991201	TW 97105488	A	19970426	200042
US 6133978	A	20001017	US 97847808	A	19970425	200054
KR 246020	B1	20000302	KR 9715782	A	19970426	200122
US 6396557	B1	20020528	US 97847808	A	19970425	200243
			US 2000651570	A	20000828	

Priority Applications (No Type Date): JP 96108288 A 19960426

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 803906	A2	E	23	H01L-023/498	
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Designated States (Regional): DE FR GB

JP 9292624	A	11	G02F-001/1345
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KR 97072373	A		H01L-023/52
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TW 375694	A		G02F-001/133
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US 6133978	A		G02F-001/133
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KR 246020	B1		H01L-023/52
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US 6396557	B1		G02F-001/133	Div ex application US 97847808
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Div ex patent US 6133978

Abstract (Basic): EP 803906 A

The liquid crystal display device has a number of tape carrier packages (TCP) mounted on it to connect its driving **semiconductor chips**. The packages are formed on a large **insulating film** and have **conductive** patterns formed on it or adhered to it. Openings are provided for the chips and through holes have **conductors** bent into them. The chip (4) has **conductive bumps** (9) that mate with the through holes for connection to the leads (3')

The chip and its connections are covered by an anisotropic resin (5). Discrete components can be added before the resin is applied. **Conductive** particles can be added to the resin in the form of 3 micrometre gold coated balls.

ADVANTAGE - Provides simple construction for package and allows it to be tested readily.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/26/2002 09/939,457

52/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011430707

WPI Acc No: 1997-408614/199738

XRPX Acc No: N97-340031

Semiconductor package mfg method e.g. for electronic device - by pushing whole **semiconductor chip** against carrier film and then performing electrical bonding of pad and **electrode**, followed by thermocompression bonding to form external **electrode**

Patent Assignee: SUMITOMO METAL MINING CO (SUMM)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9181117	A	19970711	JP 95338491	A	19951226	199738 B

Priority Applications (No Type Date): JP 95338491 A 19951226

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 9181117	A	7		

Abstract (Basic): JP 9181117 A

The method involves forming an **insulating layer**, a wiring **layer** and a binding material layer such that the binding material layer touches the **semiconductor chip**. A carrier film is arranged opposing the **bump electrode** of the **electrode** pad on the chip. The carrier film is set such that the **bump electrode** is turned to the heat stage. A tool with the flat end is used to absorb the chip such that the **electrode** pad is turned to the lower side. The chip is pushed against the carrier film.

Load and temperature are applied to the **electrode** pad and **bump electrode**, thereby performing electrical bonding of the pad and **electrode**. Further more, this tool is dropped and the adhesive agent layer of the carrier film contacts the surface of the chip. Thermocompression bonding is performed and an external **electrode** is formed. The carrier film is then cut.

ADVANTAGE - Prevents generation of air bubbles between **semiconductor chip** and adhesive agent layer of carrier film, as crimp is performed continuously. Requires only one process for sealing by electrical bonding.

Dwg.1/3

09/26/2002 09/939,457

52/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011273395

WPI Acc No: 1997-251298/199723

XRAM Acc No: C97-081079

XRPX Acc No: N97-207725

Semiconductor device with tape carrier package - in which 2-D
electrodes are projected from surface opposite to chip comparison
surface of film substrate

Patent Assignee: SONY CORP (SONY)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9082752	A	19970328	JP 95236566	A	19950914	199723 B

Priority Applications (No Type Date): JP 95236566 A 19950914

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 9082752	A	5	H01L-021/60	

Abstract (Basic): JP 9082752 A

The **semiconductor** device includes a **bump electrode** (4) formed on an array of **electrode** pads (3). A **semiconductor chip** (1) is mounted onto the **bump electrode**. An **insulated film** (5) serves as base material, into which a slit (6) is formed. The opening is performed by punching the **insulated film**, at position corresponding to the **electrode** formation in the chip.

A film substrate (2) with wiring pattern (7), is provided at the under surface of the chip. The **bump electrode** of the **semiconductor chip** is connected to the wiring pattern, through the slit. Several 2D **electrodes** (8) are projected from surface opposite to chip comparison surface of the film substrate.

ADVANTAGE - Improves mounting efficiency. Applies to PCB, device high mounting density is realised. Prevents increase in appts size. Expands entire in plane area of film substrate.

Dwg.1/5

09/26/2002 09/939,457

52/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010504345

WPI Acc No: 1996-001296/199601
Related WPI Acc No: 1999-622215
XRAM Acc No: C96-000496
XRPX Acc No: N96-001100

Mfr. of a bump leaded film carrier **semiconductor** device - by
adhering a chip to an **insulating film** through to bumps on the
other side and locally pressing to bond the **conductive** pattern to
pads on the chip

Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE)

Inventor: HAGIMOTO E; KATA K; MATSUDA S

Number of Countries: 007 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 684644	A1	19951129	EP 95108029	A	19950524	199601 B
JP 7321157	A	19951208	JP 94110857	A	19940525	199607
US 5683942	A	19971104	US 95450728	A	19950525	199750
JP 10074807	A	19980317	JP 94110857	A	19940525	199821
			JP 97208716	A	19940525	
US 5905303	A	19990518	US 95450728	A	19950525	199927
			US 97873593	A	19970612	
KR 203030	B1	19990615	KR 9513222	A	19950525	200061
EP 684644	B1	20020206	EP 95108029	A	19950524	200211
			EP 99115292	A	19950524	
DE 69525280	E	20020321	DE 625280	A	19950524	200227
			EP 95108029	A	19950524	

Priority Applications (No Type Date): JP 94110857 A 19940525; JP 97208716 A 19940525

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 684644	A1	E	36	H01L-023/31	
Designated States (Regional): DE FR GB NL					
JP 7321157	A		14	H01L-021/60	
US 5683942	A		32	H01L-021/60	
JP 10074807	A		13	H01L-021/60	Div ex application JP 94110857
US 5905303	A			H01L-023/48	Div ex application US 95450728
					Div ex patent US 5683942
KR 203030	B1			H01L-021/60	
EP 684644	B1	E		H01L-023/31	Related to application EP 99115292
					Related to patent EP 959499
Designated States (Regional): DE FR GB NL					
DE 69525280	E			H01L-023/31	Based on patent EP 684644

Abstract (Basic): EP 684644 A

Semiconductor device is mfd. by forming an **insulating**
film (3) with **conductive layers** (6) on one surface
and **conductive bumps** (9) on the other surface connected to

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the **conductive layers** through the **film**, bonding a chip (1) on the other surface connected to the **conductive layers** through the **film**, bonding a chip (1) with pads (2) to the film via adhesive (22), and locally pressing so that the **conductive layers** are connected to the pads.

Semiconductor device mfd. as above is claimed. Also claimed is a flexible film for mounting a chip (1) with pads (2) comprising an **insulating film** with **conductive layers** (6) on one side and **conductive bumps** (9) on the other side, **conductive vias** (4) inserted in holes in the film to connect layers (6) to bumps (4), and openings (21) in the film for locally pressing the **conductive layers** (6) onto the pads (2).

ADVANTAGE - Combination of chip, film and thin adhesive layer results in a firm yet small device.

Dwg.5/20

Abstract (Equivalent): US 5683942 A

A method for manufacturing a **semiconductor** device, comprising the steps of:preparing an **insulating film** having a first surface on which **conductive layers** are formed and a second surface on which **conductive** protrusions connected through the **insulating film** to respective ones of the **conductive layers** are formed, the **insulating film** also having openings through it, the openings being covered with respective the **conductive layers**,preparing a **semiconductor chip** having pads located opposite respective the openings and a passivation film located so that the pads are surrounded by the passivation film, a surface of the pads being less distant from the **semiconductor chip** than a surface of the passivation film,

adhering the **semiconductor chip** to the **insulating film** by an adhesive layer so that the openings oppose respective the pads through respective the **conductive layers**, and locally bending the **conductive layers** by inserting a bonding tool into the openings and pressing the **conductive layers** with the bonding tool, thereby electrically connecting the **conductive layers** with respective the pads.

Dwg.7H/20

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52/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009978659

WPI Acc No: 1994-246372/199430

XRFX Acc No: N94-194609

Manufacture of **semiconductor** device for lap-tops and **portable**
personal computer - reduces thermal resistance of tape carrier package
carrying out surface note resin sealing and joining metal board to
back side.

Patent Assignee: HITACHI CHO LSI ENG KK (HISC); HITACHI LTD (HITA);
HITACHI MICON SYSTEM KK (HITA-N)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 6181236	A	19940628	JP 92334342	A	19921215	199430 B

Priority Applications (No Type Date): JP 92334342 A 19921215

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6181236	A		4	H01L-021/60	

Abstract (Basic): JP 6181236 A

The **semiconductor** integrated circuit device has a tape
carrier package (10) structure, connected to the lead (2) end of the
semiconductor chip (4) placed on the surface of an
insulation film (1). The **insulation film** is
projected inside a device hole through the **bump electrode**
(5). The tape carrier package is joined to the metal board (7) at the
back side of **semiconductor chip** and sealed on the surface
side by resin (8).

The tape carrier package is manufactured by transfer mould method.
For this a metal die, with the **semiconductor chip** joined to
metal board at back and sealed with resin at the surface, is shaped.

ADVANTAGE - Reduced thermal resistance tape carrier package, of
reduced thermal. High yield of tape carrier package.

Dwg.1/2

09/26/2002 09/939,457

52/3,AB/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009842299

WPI Acc No: 1994-122155/199415

XRFX Acc No: N94-261806

Tape carrier package type **semiconductor** device capable of preventing crosstalk - has **semiconductor chip** disposed in hole made in **insulating film**, and wiring pattern having leads formed on one of top and bottom surfaces of **insulating film**, each with lead connected to chip

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: IKEMIZU M; OKUTOMO T

Number of Countries: 003 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 6069275	A	19940311	JP 92328893	A	19921114	199415 B
US 5359222	A	19941025	US 9311133	A	19930129	199442
US 5659198	A	19970819	US 9311133	A	19930129	199739
			US 94212875	A	19940315	
			US 95539737	A	19951005	
KR 9704217	B1	19970326	KR 931224	A	19930130	199937

Priority Applications (No Type Date): JP 9217097 A 19920131

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6069275	A		12	H01L-021/60	
US 5359222	A		17	H01L-023/48	
US 5659198	A		18	H01L-023/552	Div ex application US 9311133 Cont of application US 94212875 Div ex patent US 5359222
KR 9704217	B1			H01L-021/60	

Abstract (Basic): JP 6069275 A

Dwg.1/22

US 5359222 A

The inner lead portion of each of the leads is bonded to a corresp one of **bump electrodes** formed on pads of a **semiconductor chip** and the outer lead portion thereof is connected to a corresp lead wire formed on a printed circuit board. The outer lead portion of one of the leads which acts as a ground line is connected to a grounded lead wire which is formed on the printed circuit board. An insulating adhesive agent bonds a shield plate to the under surface of the wiring pattern.

The **semiconductor chip** is mounted on a base plate having a number of lead wires connected to the outer lead portions. At least one of the number of lead wires is grounded and electrically connected to the shield plate. The lower surface of the shield plate and the connections of the lead wires to the outer lead portions are in the same plane. The **semiconductor chip** and the inner lead portions are hermetically sealed by use of potting resin.

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USE/ADVANTAGE - Provides TCP or TAB type **semiconductor** device, exhibiting excellent HF characteristic and facilitates increase in number of pins used, miniaturisation and flatness of carrier tape.

Dwg.1/17

Abstract (Equivalent): US 5659198 A

A **semiconductor** device comprising:

a **semiconductor chip**;

an **insulating film** defining a position for said **semiconductor chip** and having an under surface;

a wiring pattern on said under surface of said **insulating film** and having leads each including an inner lead portion connected to said **semiconductor chip** and an outer lead portion extending from said inner lead portion;

a metal plate facing said under surface of said **insulating film**; and

an insulating adhesive agent inserted between said under surface of said **insulating film** and said metal plate, said insulating adhesive agent burying said inner lead portions of said wiring pattern by covering contiguous portions of three adjacent surfaces of each of said inner lead portions.

Dwg.1/17

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52/3,AB/18 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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06309750

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 11-251348 [JP 11251348 A]
PUBLISHED: September 17, 1999 (19990917)
INVENTOR(s): SHIMOISHIZAKA NOZOMI
SAWARA RYUICHI
NAKAMURA YOSHIFUMI
KUMAGAWA TAKAHIRO
APPLICANT(s): MATSUSHITA ELECTRON CORP
APPL. NO.: 10-050343 [JP 9850343]
FILED: March 03, 1998 (19980303)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a smaller **semiconductor** device, which is positively connected with an external device, at **lower cost** without the need for a metal line, a resin substrate, and a metal ball.

SOLUTION: A main surface of a **semiconductor chip** 10 is provided with an **insulating layer** 20 which has openings disposed above **electrodes** 11 and protrusions 22 disposed at anywhere other than the openings, **protruding electrodes** 32 disposed on the protrusions 22 so as to be connected with an external device, metal wires 31 for connecting the **protruding electrodes** 32 to pads 30 connected with the **electrodes** 11, and a solder resist 50 which is formed so as to cover portions other than the **protruding electrodes** 32 on the main surface. Instead of a metal line, a resin substrate, and a metal ball, it is possible to use the metal wires 1 and the **protruding electrodes** 32 which are disposed on the **insulating layer** 20. Thus, a smaller **semiconductor** device, which is positively connected with the external device, can be achieved at **lower material cost**.

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52/3,AB/19 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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03264127
FORMATION OF **ELECTRODE OF SEMICONDUCTOR CHIP**

PUB. NO.: 02-239627 [JP 2239627 A]
PUBLISHED: September 21, 1990 (19900921)
INVENTOR(s): MATSUZAKI KAZUO
APPLICANT(s): FUJI ELECTRIC CO LTD [000523] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-060111 [JP 8960111]
FILED: March 13, 1989 (19890313)
JOURNAL: Section: E, Section No. 1011, Vol. 14, No. 557, Pg. 49, December 11, 1990 (19901211)

ABSTRACT

PURPOSE: To enable formation of an **electrode** of a **semiconductor chip** which enables multiple piling by providing a **bump electrode** and a through **bump electrode** to the **semiconductor chip**.

CONSTITUTION: A silicon substrate 5 is set to an anode, an inner wall surface of a through hole 13 is anode-oxidized and an **insulating film** (SiO(sub 2)) 14 is formed. Thereafter, a polarity is changed to **carry** out electric plating in a solder plating solution and to bury a solder 15 into the through hole 13. A photoresist 12 in an upper side of a Cu layer 11b is selectively removed. Ni plating of 0.2.mu.m thickness is applied to a surface of the solder 15 buried in the through hole 13 and a surface of the Cu layer 11b, respectively using a remaining resist as a mask to acquire Ni plated layers 16a and 16b. Solder plated layers 17a and 17b are successively formed in a thickness of about 50.mu.m to each of the Ni plated layers 16a and 16b. Then, the resist 12 is removed for solder reflow, and the solder plated layer 17a is formed into a through **bump electrode** 18 and the solder plated layer 17b is formed into a **bump electrode** 19. Thereby, **semiconductor chips** can be piled readily.

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57/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014077826

WPI Acc No: 2001-562040/200163

XRPX Acc No: N01-418149

Flip-chip mounting type **semiconductor** device for
portable electronic device, has resilient electroconductive
connection layer, connecting circuit board with
semiconductor device

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001217281	A	20010810	JP 200021668	A	20000131	200163 B

Priority Applications (No Type Date): JP 200021668 A 20000131

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001217281	A	10	H01L-021/60	

Abstract (Basic): JP 2001217281 A

Abstract (Basic):

NOVELTY - A **bump electrode** (4) and a resilient
electroconductive **connection layer** (8) **connect** the
circuit board (6) with the **semiconductor** device (1).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for
semiconductor device manufacturing method.

USE - For **portable electronic** device.

ADVANTAGE - The **connection** layer due to its resiliency
restrains the height variation of the **bump electrode** and
variations in the flatness of **circuit board** and reduces
need for a heavy load for pressing the **semiconductor** device.
Prevents the damage to the **semiconductor** device and **circuit**
board during mounting process and provides a stable, reliable
electric **connection** between **semiconductor** device and
circuit board.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of
semiconductor device structure.

Semiconductor device (1)

Bump electrode (4)

Circuit board (6)

Resilient electroconductive **connection** layer (8)

pp; 10 DwgNo 1/12

09/26/2002 09/939,457

57/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014044753

WPI Acc No: 2001-528966/200158
Related WPI Acc No: 2001-410362
XRAM Acc No: C01-157706
XRPX Acc No: N01-392574

Flexible wiring board for use in liquid crystal display devices,
comprises thin **polymer** film which is rendered freely bendable in
the vicinity of **semiconductor chip** mounting region
Patent Assignee: CASIO COMPUTER CO LTD (CASK); CASIO MICRONICS KK (CASK
); SAITO H (SAIT-I)

Inventor: SAITO H

Number of Countries: 004 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010009299	A1	20010726	US 2001766269	A	20010119	200158 B
JP 2001210676	A	20010803	JP 200016492	A	20000126	200159
JP 2001284751	A	20011012	JP 2000372946	A	20001207	200176
CN 1316871	A	20011010	CN 2001102313	A	20010131	200207
KR 2001078040	A	20010820	KR 20013501	A	20010122	200212
US 6433414	B1	20020813	US 2001766269	A	20010119	200255

Priority Applications (No Type Date): JP 2000372946 A 20001207; JP
200016491 A 20000126; JP 200016492 A 20000126

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010009299	A1		21	H01L-023/48	
JP 2001210676	A		6	H01L-021/60	
JP 2001284751	A		10	H05K-001/02	
CN 1316871	A			H05K-001/00	
KR 2001078040	A			G02F-001/1345	
US 6433414	B1			H01L-023/06	

Abstract (Basic): US 20010009299 A1

Abstract (Basic):

NOVELTY - A flexible wiring board comprises a thin **polymer**
film which is rendered freely bendable in the vicinity of a
semiconductor chip mounting region.

DETAILED DESCRIPTION - A flexible wiring board for **connection**
to an electronic part comprises:

- (a) a film (47);
- (b) **connection** terminals (45a, 45b) electrically arranged in
the **connection** terminal region of the film; and
- (c) drawing wirings (45c) which electrically **connect** the
connection terminals and the **semiconductor chip** (43).

The film has a **semiconductor chip** mounting region, a
connection terminal region, and an inclined wiring region, which
is to be bent freely and positioned between the **connection**
terminal region and the **semiconductor chip** mounting region.
The drawing wiring has an inclined wiring section that is to be bent

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freely, and arranged in the inclined wiring region of the film.

INDEPENDENT CLAIMS are also included for:

(A) a display device comprising (i) the flexible wiring board and (ii) a display panel (31) electrically **connected** to the **connection** terminals of the flexible wiring board; and

(B) a method of manufacturing a flexible wiring board **connected** to a **semiconductor chip**, comprising:

(i) heating one surface of the **semiconductor chip**,
(ii) aligning metallic-made **bump electrodes** arranged on the opposite surface of the **semiconductor chip** with the **connection** terminals formed on one surface of the flexible wiring board, and

(iii) applying a pressure while heating an opposite surface of the flexible wiring board to bond the **bump electrodes** to the **connection** terminals.

USE - In electronic parts, e.g. liquid crystal display devices.

ADVANTAGE - Since the **connection** terminals are formed to include inclined regions positioned to be gradually apart from the **semiconductor chip** together with the film substrate from the portions bonded to the **bump electrodes** toward the outside of the mounting region of the **semiconductor chip**, it is possible to prevent the number of manufacturing steps from being increased. Since a bonding tool is brought into direct contact with the other surface of the film substrate under certain conditions with the **semiconductor chip** kept heated so as to pressurize the **semiconductor chip** under heat, a bonding of high reliability is obtained, even where the film substrate has one surface corresponding to one surface of the **semiconductor chip** over the entire mounting region of the **semiconductor chip** and other surfaces. Since a device hole is not formed in the **semiconductor chip** mounting region of the film substrate, it is possible to prevent the **connection** terminals mounted to the film substrate from being deformed. The flexible wiring board can be bent easily in the vicinity of a **semiconductor chip** mounting region without forming slits for facilitating the bending in the film substrate, thus it is possible to decrease the length of that portion of the flexible wiring board that is positioned ahead of the **semiconductor chip** mounting region. It can also be miniaturized while maintaining a good **connection** and can be made excellent in the mounting capability with a high mounting density. Manufacturing **cost** can be **lowered**.

DESCRIPTION OF DRAWING(S) - The figure shows a view of a liquid crystal display module mounted to a **circuit board**.

Display panel (31)

Semiconductor chip (43)

Connection terminals (45a, 45b)

Drawing wirings (45c)

Film (47)

pp; 21 DwgNo 4/14

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57/3,AB/3 (Item 3 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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013884785

WPI Acc No: 2001-368998/200139

XRAM Acc No: C01-113283

XRPX Acc No: N01-269318

Mounting of **semiconductor chip** on **circuit board**
for manufacturing electromagnetic wave readable data carrier, involves
melting **thermoplastic resin coat** of **circuit**
board and applying ultrasonic wave

Patent Assignee: OMRON CORP (OMRO); OMRON KK (OMRO); KAWAI W (KAWA-I)

Inventor: KAWAI W

Number of Countries: 030 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1104017	A2	20010530	EP 2000310393	A	20001123	200139 B
JP 2001156110	A	20010608	JP 99333409	A	19991124	200148
CN 1300180	A	20010620	CN 2000128333	A	20001124	200159
KR 2001070230	A	20010725	KR 200069772	A	20001123	200206
US 6406990	B1	20020618	US 2000716289	A	20001121	200244
US 20020115278	A1	20020822	US 2000716289	A	20001121	200258
			US 2002122317	A	20020416	

Priority Applications (No Type Date): JP 99333409 A 19991124

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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EP 1104017	A2	E 29	H01L-021/60	
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Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI TR

JP 2001156110	A	17	H01L-021/60
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CN 1300180	A		H05K-003/00
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KR 2001070230	A		H01L-023/28
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US 6406990	B1		H01L-023/48
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US 20020115278	A1		H01L-021/44	Div ex application US 2000716289
				Div ex patent US 6406990

Abstract (Basic): EP 1104017 A2

Abstract (Basic):

NOVELTY - A **semiconductor chip** is mounted on
circuit board by melting a **thermoplastic resin**
coat of **circuit board**. A bump (9) of
semiconductor chip is caused to penetrate the melted
resin coat and contact with **electrode** area (10) by
applying an ultrasonic wave to it. The **bump** and **electrode**
area are bonded by continuously applying the ultrasonic wave. The
melted resin is then cooled and solidified.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for (A)
a **circuit board** (7) for a flip-chip **connection**; (B) a
method of manufacturing **circuit board**; and (C) an
electromagnetic wave readable data carrier. The **circuit**
board comprises a wiring pattern (6) disposed on a thin base

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material, and a **thermoplastic resin coat** (4a). The **resin coat** acts as a mask for forming the wiring pattern by etching process. The **circuit board** is manufactured by laminating a metal foil on thin base material, forming a **resin coat** on metal foil, and etching a portion of metal foil where the **resin coat** is not formed. The electromagnetic wave readable data carrier comprises a body of data carrier including a **conductive** pattern held on an insulating base material.

USE - For manufacturing an electromagnetic wave readable data carrier useful as e.g., flight tag, label for physical distribution management, or ticket for an unmanned wicket.

ADVANTAGE - The inventive method provides a **semiconductor chip** (8), which is promptly, electrically, and mechanically secured on a **circuit board** at low cost. The melting step provides a sealed structure of satisfactory moisture-proof, and bonded structure of high tensile strength.

DESCRIPTION OF DRAWING(S) - The drawing shows an ultrasonic mounting process of the inventive method.

Thermoplastic resin coat (4a)

Wiring pattern (6)

Circuit board (7)

Semiconductor chip (8)

Bump (9)

Electrode area (10)

pp; 29 DwgNo 1D/15

09/26/2002 09/939,457

57/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013518806

WPI Acc No: 2001-003012/200101

XRPX Acc No: N01-002613

Semiconductor chip connection procedure involves
connecting bump electrode to electrode terminal
of **printed circuit board** after heating and softening of
anisotropic **conductive resin layer**

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000286299	A	20001013	JP 9988743	A	19990330	200101 B

Priority Applications (No Type Date): JP 9988743 A 19990330

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000286299	A		5 H01L-021/60	

Abstract (Basic): JP 2000286299 A

Abstract (Basic):

NOVELTY - The **bump electrode** (2) of a
semiconductor chip (1) is **connected** to the
electrode terminal (8) of a **printed circuit**
board (7) after heating and softening of an anisotropic
conductive resin layer (9). The **semiconductor**
chip is pressed directly to the **printed circuit**
board.

USE - For **semiconductor chip** used in e.g.
notebook computer, portable telephone.

ADVANTAGE - Increases operating efficiency of **semiconductor**
chip. Uses **resin layer** with uniform thickness.
Simplifies formation of **bump electrodes**. Ensures strong and
reliable **connection** that can withstand expansion contraction of
resin. Secures reliability of bonding strength and **connection**.

DESCRIPTION OF DRAWING(S) - The figure shows the mounting process
sectional view of a **semiconductor chip**.

Semiconductor chip (1)

Bump electrode (2)

Printed circuit board (7)

Electrode terminal (8)

Anisotropic conductive resin layer (9)

pp; 5 DwgNo 1/2

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57/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012553699

WPI Acc No: 1999-359805/199931

XRAM Acc No: C99-106652

XRPX Acc No: N99-268023

Plastic **semiconductor** package has a structure that improves its heater diffusibility especially in case of moisture absorption
Patent Assignee: MITSUBISHI GAS CHEM CO INC (MITN); GAKU M (GAKU-I);
IKEGUCHI N (IKEG-I); YAMANE N (YAMA-I)

Inventor: GAKU M; IKEGUCHI N; YAMANE K; YAMANE N

Number of Countries: 029 Number of Patents: 022

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6376908	B1	20020423	US 98207115	A	19981208	200232
US 20020100967	A1	20020801	US 98207115	A	19981208	200253
			US 200236385	A	20020107	

Priority Applications (No Type Date): JP 9838917 A 19980220; JP 97340129 A 19971210; JP 98975 A 19980106; JP 983984 A 19980112; JP 984835 A 19980113 ; JP 984836 A 19980113; JP 989567 A 19980121; JP 989568 A 19980121; JP 9811528 A 19980123; JP 9815893 A 19980128; JP 9817045 A 19980129; JP 9834232 A 19980130; JP 9834233 A 19980130; JP 9834234 A 19980130; JP 9834235 A 19980130; JP 9834236 A 19980130; JP 9834238 A 19980130

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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EP 926729	A2	E 40	H01L-023/13	
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Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI

US 6376908	B1	H01L-023/10
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US 20020100967	A1	H01L-023/10	Div ex application US 98207115
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Abstract (Basic): EP 926729 A2

Abstract (Basic):

NOVELTY - Plastic **semiconductor** package has novel structure improving its heat diffusibility and durability, and preventing occurrence of the bubbling 'popcorn phenomenon'.

DETAILED DESCRIPTION - Plastic **semiconductor** package is made by fixing **semiconductor chip** on one surface of **printed circuit board**, **connecting semiconductor circuit conductor** to signal propagation circuit **conductor A** formed in its vicinity on a **printed circuit board** surface by wire bonding, at least **connecting the conductor A** to a signal propagation circuit **conductor B** formed on the other surface of the **printed circuit board**, or a **connecting conductor** pad of a solder ball with a through-hole **conductor** (preferably through a blind via-conduction hole formed on the side of the **printed circuit board** surface), and encapsulating the **semiconductor chip** with resin. The **printed circuit board** has a metal sheet of nearly same size as the

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

board, nearly in the center in the thickness direction of the **printed circuit board**, the metal sheet being insulated from **front** and reverse circuit **conductors** with a heat-resistant resin composition, and the metal plate is provided with a clearance hole of diameter greater than that of each of at least two through-holes being provided in the clearance hole and insulated from the metal sheet with a resin composition. At least one through-hole is **connected** to the metal sheet and one surface of the metal sheet has at least one protruding area of the same size as that of the **semiconductor chip** and exposed on the surface, with the **semiconductor chip** fixed on this protruding area (while the other side of the metal sheet has preferably exposed protrusion area for diffusing heat). An INDEPENDENT CLAIM is also included for the process of production of double-sided metal foil-clad laminate for plastic **semiconductor** package, comprising:

(1) forming protrusion on one surface of the metal sheet for mounting of the **semiconductor chip**, forming clearance hole with diameter greater than that of the through-hole, or a slit whose smaller side is greater than the diameter of the through-hole, providing hole for **front** and reverse circuit **conductors**;

(2) providing low-flow or no-flow prepreg sheet or **resin layer** with a hole slightly greater than the metal protrusion area, with high-flow prepreg sheet or **resin layer** having sufficient **resin** flow to fill clearance hole on the other side, and providing metal foil or single-side metal foil-clad laminates on both outer sides; and

(3) laminate-forming, under heat and pressure, to integrate it with inserted metal sheet, and produce dual-side metal foil-clad laminate.

USE - In production of **semiconductor** devices.

ADVANTAGE - The package has excellent heat diffusibility and heat durability, especially in case of moisture absorption.

DESCRIPTION OF DRAWING(S) - The drawing shows producing plastic **semiconductor** package.

- liquid etching resist (a)
 - metal sheet (b)
 - negative film (c)
 - clearance hole (d)
 - metal foils (e)
 - low-flow prepreg (f)
 - high-flow prepreg (g)
 - through hole (h)
 - semiconductor chip** (j)
 - electro- or thermo-**conductive** adhesive (k)
 - wire bonding (l)
 - resin (m)
 - solder ball (n)
- pp; 40 DwgNo 1/12

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57/3,AB/6 (Item 6 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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012306128

WPI Acc No: 1999-112234/199910

XRPX Acc No: N99-082105

Resin sealed package **semiconductor** device e.g. for mask-ROM card,
IC card - has insulating sheet of fixed thickness which is arranged
between **semiconductor chip** and **circuit board**

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10335578	A	19981218	JP 97147925	A	19970605	199910 B

Priority Applications (No Type Date): JP 97147925 A 19970605

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 10335578	A	5	H01L-025/065	

Abstract (Basic): JP 10335578 A

NOVELTY - An **electrode** pad (16) of a **semiconductor chip** (12) is **connected** to a **connection** pad (19) of a **circuit board** (13) through a solder bump (17). A polyimide resin made insulating sheet (18) of fixed thickness is arranged between the **semiconductor chip** and **circuit board**.

USE - For mask-ROM card, IC card, game machine, **portable** telephone.

ADVANTAGE - Predetermined insulation gap is secured between solder bumps thereby preventing the crushing of solder bump during soldering process. Improves reliability of device. Facilitates miniaturisation of device. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of **semiconductor** device. (12) **Semiconductor chip**; (13) **Circuit board**; (16) **Electrode** pad; (17) Solder bump; (18) Insulating sheet; (19) **Connection** pad.

Dwg.1/4

09/26/2002 09/939,457

57/3,AB/7 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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04678073
RESIN-SEALED **SEMICONDUCTOR** DEVICE

PUB. NO.: 06-349973 [JP 6349973 A]
PUBLISHED: December 22, 1994 (19941222)
INVENTOR(s): NISHINO TOMONORI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 05-142212 [JP 93142212]
FILED: June 14, 1993 (19930614)

ABSTRACT

PURPOSE: To provide a resin-sealed **semiconductor** device low in cost an in the prior art, but having large heat dissipating amount, adaptable for a high density surface mount for transmitting a high speed signal, with high performance such as a **small** size.a light **weight**.

CONSTITUTION: The resin-sealed **semiconductor** device comprises a **semiconductor chip** 1 provided with alloy **protruding electrodes** on a main surface, and a **circuit board** 11 electrically **connected** to the chip in such a manner that the chip 1 is resin-sealed, and an alloy protruding terminal 13 provided on the other surface of the board 11.

09/26/2002 09/939,457

59/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014646091

WPI Acc No: 2002-466795/200250

XRPX Acc No: N02-367948

Semiconductor chip mounting structure for **electronic**
device e.g. **portable** telephone, has several pads on multilayer
wiring board whose corner end portion are arc-shaped or inclined

Patent Assignee: CASIO COMPUTER CO LTD (CASK)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2002110712	A	20020412	JP 2000292153	A	20000926	200250 B

Priority Applications (No Type Date): JP 2000292153 A 20000926

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2002110712	A	10	H01L-021/56	

Abstract (Basic): JP 2002110712 A

Abstract (Basic):

NOVELTY - An underfilling (16) is filled between a
semiconductor chip (14) and a multilayer wiring board after
the **connection** of **bump electrodes** of the chip with
the pads (20) on the wiring board. The end portion (21) at the corners
of the pads is arc-shaped or inclined.

USE - **Semiconductor chip** mounting structure for
electronic device such as **portable** telephone, wrist watch,
etc.

ADVANTAGE - By having the inclined or arc-shaped corner end
portions for the pad, underfilling enters smoothly between
semiconductor chip and wiring board, even when the gap
between each pad is narrow, thus firmly and reliably fixing the chip on
the wiring board.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged plan view
of condition of having removed the **semiconductor chip**.

Semiconductor chip (14)

Underfilling (16)

Pads (20)

End portion (21)

pp; 10 DwgNo 2/20

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59/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014604659

WPI Acc No: 2002-425363/200245

XRPX Acc No: N02-334486

Semiconductor device for **portable**, small/densely mounted devices, comprises metal plate arranged on exposed portion of heat radiation **electrode**, to **protrude** beyond back surface of pad provided over **semiconductor chip**

Patent Assignee: SANYO ELECTRIC CO LTD (SAOL); IGARASHI Y (IGAR-I); KOBAYASHI Y (KOBAY-I); MAEHARA E (MAEH-I); OKADA Y (OKAD-I); SAKAMOTO J (SAKA-I); SAKAMOTO N (SAKA-I); TAKAHASHI K (TAKA-I)

Inventor: IGARASHI Y; KOBAYASHI Y; MAEHARA E; OKADA Y; SAKAMOTO J; SAKAMOTO N; TAKAHASHI K

Number of Countries: 029 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020041023	A1	20020411	US 2001810141	A	20010316	200245 B
EP 1199746	A2	20020424	EP 2001302527	A	20010320	200245
CN 1348214	A	20020508	CN 2001117311	A	20010210	200253
JP 2002184912	A	20020628	JP 2001240542	A	20010808	200258

Priority Applications (No Type Date): JP 2000306669 A 20001005

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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US 20020041023	A1		26	H01L-023/36	
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EP 1199746	A2	E		H01L-023/31	
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Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI TR

CN 1348214	A			H01L-023/34	
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JP 2002184912	A		21	H01L-023/34	
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Abstract (Basic): US 20020041023 A1

Abstract (Basic):

NOVELTY - A metal plate (23) is arranged on an exposed portion of a heat radiation **electrode** (15), to **protrude** beyond the back surface of a pad. The pad is electrically **connected** to a bonding **electrode** of a **semiconductor chip**, to expose the back side of an insulating resin that molds the **semiconductor chip** integrally in a face-down state.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(a) **Semiconductor** module; and

(b) Hard disk comprising **semiconductor** device.

USE - For **portable**, small/densely mounted devices such as hard disk (claimed).

ADVANTAGE - The metal plate in combination with the radiation **electrode**, efficiently dissipates the heat generated by the **semiconductor chip**. Increases read/write operation of hard disk by enabling efficient external emission of heat.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional

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diagram of the **semiconductor** module.

Heat radiation **electrode** (15)

Metal plate (23)

pp; 26 DwgNo 1B/18

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59/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014398683

WPI Acc No: 2002-219386/200228

XRAM Acc No: C02-067209

XRPX Acc No: N02-168138

Electronic component assembling method involves resin sealing all unit areas of substrate mounted with **semiconductor chips** and placing on test board for simultaneous testing

Patent Assignee: TOWA KK (TOWA-N); TOWA CORP (TOWA-N)

Inventor: NAKAGAWA O; TAKEHARA M

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001135658	A	20010518	JP 99316209	A	19991108	200228 B
US 6358776	B1	20020319	US 2000705239	A	20001102	200228
KR 2001070191	A	20010725	KR 200065501	A	20001106	200228

Priority Applications (No Type Date): JP 99316209 A 19991108

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001135658	A		8	H01L-021/56	
US 6358776	B1			H01L-021/44	
KR 2001070191	A			H01L-023/552	

Abstract (Basic): JP 2001135658 A

Abstract (Basic):

NOVELTY - A chip (2) is mounted on each unit area (7) of substrate (1). Lateral **electrodes** (18,5) of respective chip and substrate, are electrically **connected**. The unit areas of substrate are then sealed with a sealing resin (8) and the arrangement is placed on a test board (10) for testing the electronic component. The sealed unit areas of substrate are then isolated.

DETAILED DESCRIPTION - A bump is formed on the exterior **electrode** (19) in the sealed over areas of substrate. While sealing the unit areas of substrate with resin, the substrate is mounted on mold mating face of metallic mold set consisting of pair of opposing lower and upper type metallic molds (20,21). While testing the electronic component operation, the substrate is maintained at preset temperature atmosphere. The metallic mold set is clamped to form a cavity (24) through which fused resin is injected and hardened to form sealing resin (8). The pressure inside the cavity is reduced through exhaust tube (25). After testing is completed, each unit area of substrate is separated. An INDEPENDENT CLAIM is also included for electronic component assembly apparatus which includes a tool (3) for mounting each chip to each unit area of the substrate. A bump (4) is used to electrically **connect** the chip and substrate lateral **electrodes**. An injection unit injects fused resin into the cavity formed by clamping upper and lower type metallic molds of metallic mold set to enable sealing unit seal the areas of substrate. The pressure

inside the cavity is reduced by exhaust tube. An **electrode** formation unit forms a **bump** (14) on exterior **electrode** (19) of substrate to enable mounting on test board. The test board delivers and receives an electrical signal to and from the exterior **electrodes** of substrate so as to test the operation of the electronic component. A blade is used to separate each unit area of substrate sealed with resin after completion.

USE - For assembling of an **electronic** component to **carry out** burn-in testing.

ADVANTAGE - By resin sealing all the unit areas of substrate mounted with **semiconductor chips**, all the electronic components are simultaneously conveyed to an inspection apparatus and a burn-in apparatus and hence time and labor to insert and remove each electronic component is reduced. By injecting fused resin into cavity, resin sealing is performed with high dimensional accuracy. By reducing the pressure inside the cavity through exhaust tube, the generation of void in the injected fused resin is suppressed and hence the electronic component is assembled with high quality and dimensional accuracy.

DESCRIPTION OF DRAWING(S) - The figure explains the sectional drawing of electronic component assembling method. (Drawing includes non-English language text).

- Substrate (1)
- Chip (2)
- Tool (3)
- Bumps (4,14)
- Electrodes** (5,18,19)
- Unit area (7)
- Resin (8)
- Test board (10)
- Molds (20,21)

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59/3,AB/4 (Item 4 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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014027078

WPI Acc No: 2001-511292/200156

Stacked flip chip package using carrier tape
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: AHN E C; SIM J B; SONG Y J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
KR 2001017143	A	20010305	KR 9932515	A	19990809	200156 B

Priority Applications (No Type Date): KR 9932515 A 19990809

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001017143	A		1	H01L-021/58	

Abstract (Basic): KR 2001017143 A

Abstract (Basic):

NOVELTY - A stacked flip chip package using a carrier tape is provided to reduce a manufacturing cost and to shorten a manufacturing process, by flip-chip-bonding **semiconductor chips** by using a metal thin film and a carrier tape composed of an adhesion film such as an anisotropic **conductive film** or **elastomer film** having an opening which is adhered to an upper/lower surface of the metal thin film.

DETAILED DESCRIPTION - A carrier tape(150) has a metal thin film of a predetermined pattern and anisotropic **conductive films** (140). The metal thin film(130) includes bump **connecting** units(132) and beam leads(134) in both end parts. The anisotropic **conductive films** are adhered to upper and lower surfaces of the metal thin film excluding the beam leads. A plurality of **semiconductor chips**(110,120) are adhered to an upper surface of the anisotropic **conductive films** and have **bumps** while each bump corresponds to the bump **connecting** unit. The carrier tape to which the **semiconductor chips** are adhered is mounted on an upper surface of a substrate(160), and solder balls are installed on a lower surface of the substrate. A region including the carrier tape is molded with a molding resin(170). The **bump** pressures the anisotropic **conductive films** to be electrically **connected** to the bump **connecting** unit, and the beam leads are bent to be electrically **connected** to the substrate.

pp; 1 DwgNo 1/10

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59/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013200806

WPI Acc No: 2000-372679/200032

XRFX Acc No: N00-279704

Photo-**semiconductor** apparatus for multimedia apparatus, has
reflecting surface of groove which is formed at upper portion of
substrate, to transmit and receive light signal through side of contour

Patent Assignee: SANYO ELECTRIC CO LTD (SAOL)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000124478	A	20000428	JP 98295549	A	19981016	200032 B

Priority Applications (No Type Date): JP 98295549 A 19981016

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000124478	A	5	H01L-031/02	

Abstract (Basic): JP 2000124478 A

Abstract (Basic):

NOVELTY - An internal **electrode** (21) arbitrarily formed on the film substrate (20), is **connected** with light receiver (2) and light emitter (3) by bonding wire for electrification. The reflecting surface (27) of groove (26) formed on upper surface of substrate transmits or receives light signal (6) by provision of emitter or receiver correspondingly through side (24a) of contour of sealing body (24).

DETAILED DESCRIPTION - The sealing body is formed on the surface of film substrate which is provided with **bump electrode** at the rear side. A package contour is formed by **resin coating** on substrate at the side. The **semiconductor chip** formed at the side (24a) converts light signal and electrical signal.

USE - For multimedia apparatuses e.g. **notebook** PC, **portable** information terminal, **electronic** still camera.

ADVANTAGE - Since internal **electrode** is arbitrarily positioned, interference with bonding wire is prevented. Reduces mounting area of apparatus, since the chip is of leadless type.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of photo-**semiconductor** apparatus.

Light receiver (2)
Light emitter (3)
Light signal (6)
Film substrate (20)
Internal **electrode** (21)
Sealing body (24)
Side of contour (24a)
Groove (26)
Reflecting surface (27)
pp; 5 DwgNo 1/5

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59/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013091239

WPI Acc No: 2000-263111/200023

XRPX Acc No: N00-196608

Resin sealed **semiconductor** package for **portable apparatus**, has sealing resin to seal surface of **semiconductor chip**, so that surface of **bump electrodes** are exposed

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)

Inventor: OHUCHI S

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000068401	A	20000303	JP 98231894	A	19980818	200023 B
US 6107164	A	20000822	US 98184836	A	19981103	200042

Priority Applications (No Type Date): JP 98231894 A 19980818

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000068401	A	5	H01L-023/12	
US 6107164	A		H01L-021/78	

Abstract (Basic): JP 2000068401 A

NOVELTY - A **semiconductor chip** (1) has several **electrodes** (2) on its surface. A via **connects** the **electrode** (2) and **bump electrodes** (4). A sealing resin seals surface of **semiconductor chip** so that surface of **bump electrode** is exposed. A groove is formed on boundary area of chip area. Ball **electrodes** (5) are formed on surface of **bump electrodes**. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **semiconductor** package manufacturing method.

USE - In e.g. resin sealed **semiconductor** package such as **chip** size package used in **portable apparatus**.

ADVANTAGE - When dividing wafer to several pieces, the groove exposed from backside of wafer can be considered as mark, so that the wafer can be divided reliably. DESCRIPTION OF DRAWING(S) - The figure shows the manufacturing process of **semiconductor** package. (1)

Semiconductor chip; (2,4,5) Electrodes.

Dwg.1/6

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59/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012950463

WPI Acc No: 2000-122313/200011

XRPX Acc No: N00-093302

Resin sealing structure of IC card for **portable** telephone -
includes **electrode** pads on circuit formation area and pad area,
which are electrically **connected** and sealed with resin
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID); OKI DENKI KOGYO KK (OKID
)

Inventor: OHUCHI S

Number of Countries: 004 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11354580	A	19991224	JP 98160686	A	19980609	200011 B
KR 2000004851	A	20000125	KR 9836521	A	19980904	200061
TW 388975	A	20000501	TW 98114452	A	19980901	200062
US 6229222	B1	20010508	US 98140662	A	19980826	200128

Priority Applications (No Type Date): JP 98160686 A 19980609

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11354580	A		11	H01L-021/60	
KR 2000004851	A			H01L-023/28	
TW 388975	A			H01L-021/56	
US 6229222	B1			H01L-023/28	

Abstract (Basic): JP 11354580 A

NOVELTY - The **electrode** pad (4) formed on circuit formation area on the surface of **semiconductor chip** (1) is **connected** electrically with **electrode** pad (3) formed on **electrode** pad area. Resin (2) is sealed covering the **semiconductor chip** surface. A **bump electrode** (7) provided over the sealing resin is **connected** to **electrode** pad (3), electrically. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for resin sealing method of **semiconductor chip**.

USE - In IC card for **portable** telephone, **portable** game, **portable** personal computer, etc.

ADVANTAGE - By making the IC card thin, size **reduction** and **weight reduction** can be attained. DESCRIPTION OF DRAWING(S)

- The figure shows the sectional view of the IC card. (1)

Semiconductor chip; (2) Resin; (3,4) **Electrode** pads;

(7) **Bump electrode**.

Dwg.1/11

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59/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012770899

WPI Acc No: 1999-577122/199949

XRFX Acc No: N99-426279

Electrode connection structure of resin sealed
semiconductor device package - has **electrodes** on substrate
which are **connected** to respective **electrodes** of carrier tape
package through bump

Patent Assignee: SONY CORP (SONY)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11251479	A	19990917	JP 9851945	A	19980304	199949 B

Priority Applications (No Type Date): JP 9851945 A 19980304

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11251479	A	6	H01L-023/12	

Abstract (Basic): JP 11251479 A

NOVELTY - **Semiconductor chip** (3) is mounted on one side
of carrier tape (2) made of **resin film**. Several
electrodes (18) formed on the substrate are **connected** to
respective **electrodes** of carrier tape section through
conductive bumps. The **bump** and tape section are
sealed by resin material (7,14). DETAILED DESCRIPTION - Carrier tape
package is designed with larger external dimensions compared to the
size of **semiconductor chip**. An INDEPENDENT CLAIM is also
included for **semiconductor** device manufacturing method.

USE - For resin sealed **semiconductor** device package.

ADVANTAGE - As bump and carrier tape are bonded integrally and
resin, high density mounting of **semiconductor** device is achieved.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of
semiconductor device package. (2) Carrier tape; (3)

Semiconductor chip; (7,14) Resin material; (18)

Electrodes.

Dwg.1/6

09/26/2002 09/939,457

59/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012575624

WPI Acc No: 1999-381731/199932

XRFX Acc No: N99-286472

Semiconductor chip mounting procedure for **semiconductor** device used in **portable** communication **apparatus** - involves softening **bump electrodes** by heating chip to temperature below its melting point following which **bump electrodes** are made to contact **connection electrode**

Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11150152	A	19990602	JP 97316749	A	19971118	199932 B

Priority Applications (No Type Date): JP 97316749 A 19971118

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11150152	A		5	H01L-021/60	

Abstract (Basic): JP 11150152 A

NOVELTY - The **bump electrodes** (33) formed on **electrodes** (32) of a **semiconductor chip** (31) is softened by heating the chip to temperature just below the melting point of **bump electrode** and is made to contact **connection electrodes** (35). After full contact between **bump electrode** and **connection electrode** is established, chip is heated above the melting point of **bump electrode**.

USE - For **semiconductor** device used in **portable** communication **apparatus**.

ADVANTAGE - Since the **bump electrodes** are softened by heating to temperature below its melting point and are made to contact the **connection electrode**, a perfect contact between the **bump electrodes** and **connection electrodes** is established even when the **bump electrodes** vary in height, by applying small amount of pressure. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the **electrode connection** process in the **semiconductor** device manufacturing method. (31) **Semiconductor chip**; (32) **Electrodes**; (33) **Bump electrodes**; (35) **Connection electrodes**.

Dwg.1/3

09/26/2002 09/939,457

59/3,AB/10 (Item 10 from file: 350)
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011608039

WPI Acc No: 1998-025167/199803

XRAM Acc No: C98-008996

XRFX Acc No: N98-019708

Semiconductor chip mounting structure - includes
thermoplastic insulation resin in gap between **connected bump**
first **electrode**, formed by **connecting** wire board and chip

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9283555	A	19971031	JP 9694167	A	19960416	199803 B

Priority Applications (No Type Date): JP 9694167 A 19960416

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 9283555	A	5	H01L-021/60	

Abstract (Basic): JP 9283555 A

The structure includes a wiring board (35) with multiple first **electrodes** (36) onto which **semiconductor** device with bumps (33) corresponding to set of second **electrodes** (32) is mounted.

A electric **conduction** adhesive agent (34) is used to bond **bumps** and first **electrodes** thereby providing a current **carrying** part. A thermoplastic insulation resin is filled in the gap between the **connected bump** first **electrodes**.

ADVANTAGE - Improves reliability of **semiconductor** device.
Secures conductivity. Reduces size of device.

Dwg.1/5

09/26/2002 09/939,457

59/3,AB/11 (Item 11 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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011566250

WPI Acc No: 1997-542731/199750

XRPX Acc No: N97-452063

Semiconductor IC device e.g. **portable** telephone, computer
using ball grid array - has second metal plating layer of predetermined
thickness by which solder area of wiring board is electrically

connected with solder **bump electrode**

Patent Assignee: HITACHI CHO LSI ENG KK (HISC); HITACHI LTD (HITA);
HITACHI MICON SYSTEM KK (HITA-N)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9260536	A	19971003	JP 9666638	A	19960322	199750 B

Priority Applications (No Type Date): JP 9666638 A 19960322

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9260536	A		32	H01L-023/12	

Abstract (Basic): JP 9260536 A

The device has a **semiconductor chip** (1) which is fixed
on a wiring board (3) through an **elastomer layer** (2). Lead
(3L1) of wiring layer (3L) in the wiring board is electrically
connected with an external terminal (5) of the chip through a
first metal plating layer.

Solder area (3L2) of the wiring board is electrically
connected with solder **bump electrode** (3B) through a
second metal plating layer with a differing thickness from that of
first metal plating layer.

ADVANTAGE - Improves reliability and yield of **semiconductor**
device. Increases junction reliability of terminals with wiring board.

Dwg.1/48

09/26/2002 09/939,457

59/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011566149

WPI Acc No: 1997-542630/199750

XRPX Acc No: N97-451962

Semiconductor device in **portable** telephone, vehicle mounted
TV - in which **bump electrode** of **semiconductor**
chip and **connection** pad of wiring board are **connected**
by **connection** part

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9260424	A	19971003	JP 9668330	A	19960325	199750 B

Priority Applications (No Type Date): JP 9668330 A 19960325

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 9260424	A		6 H01L-021/60	

Abstract (Basic): JP 9260424 A

The device includes a **semiconductor chip** (12) mounted
on a wiring board (11). The **bump electrode** (12a) of the
chip and a **connection** pad (11a) of the board of similar size are
connected through a **connection** part (13).

A heat cured **resin layer** (14) is formed at periphery of
this **connection** part.

ADVANTAGE - Improves **connection** reliability between
semiconductor chip and PCB.

Dwg.1/10

09/26/2002 09/939,457

59/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011499500

WPI Acc No: 1997-477413/199744

XRFX Acc No: N97-398197

Surface mount type **chip** size **semiconductor** package for
portable telephone, TV - has liquefied epoxy resin filled up
between **semiconductor chip** and wiring board resulting in
formation of **resin layer**

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9223720	A	19970826	JP 9627986	A	19960215	199744 B

Priority Applications (No Type Date): JP 9627986 A 19960215

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 9223720	A	6	H01L-021/60	

Abstract (Basic): JP 9223720 A

The package includes a wiring board (11) with **connection** pad (11a) formed on its principal plane. An **electrode** pad (12a) is formed on surface of a **semiconductor chip** (12). A **bump electrode** (13) is situated between the **connection** pad of wiring board and **electrode** pad of **semiconductor chip** and a face down **connection** is carried.

A liquefied epoxy resin is filled up between the wiring board and the **semiconductor chip**. A **resin layer** (14) is thus formed along with a ridgeline (14a) on the wiring board.

ADVANTAGE - Improves mfr yield. Improves reliability.

Dwg.1/3

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59/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010584068

WPI Acc No: 1996-081021/199609

XRAM Acc No: C96-026536

XRPX Acc No: N96-067410

Ultra thin type **semiconductor** package for electronic device e.g.

LCD - has internal lead of **semiconductor chip connected**

and supported mutually with upper moulding surface of **resin**,

forming support **film** with same height as that of lead

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)

Inventor: AHN S; KIM G; MOK S

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 7321138	A	19951208	JP 95117062	A	19950516	199609 B
US 5621242	A	19970415	US 95438728	A	19950510	199721
			US 96658404	A	19960605	

Priority Applications (No Type Date): KR 9410598 A 19940516

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7321138	A		8	H01L-021/56	
US 5621242	A		8	H01L-023/50	Cont of application US 95438728

Abstract (Basic): JP 7321138 A

The ultrathin type **semiconductor** package has a **semiconductor chip** of a tape carrier, with an **electrode pad**. A number of internal and external leads (32,33) are **connected** by the **electrode pad** and **bump** of the **semiconductor chip** electrically. Between the set of internal leads, a damper (34) is formed. The **semiconductor chip** has a device hole (30) arranged on it.

The tape carrier has an injection hole (37) and a discharge mouth (38), both positioned on opposite sides of the **semiconductor chip**. A transfer moulding process is carried out, in which a resin is injected through the injection hole. The injected resin forms a moulding upper surface, **connecting** and supporting internal lead mutually, with support film height same as that of the lead.

USE/ADVANTAGE - In e.g. CR-type camera and memory card. Prevents inclination of chip on position slippage. Produces highly reliable product. Realizes **cost reduction**. Manufactures package using TAB technology, reducing high integration densities. Increases mechanical strength, even during high temperature, supporting chip and internal lead firmly. Avoids influence due to high pressure.

Dwg.1/10

Abstract (Equivalent): US 5621242 A

A **semiconductor** package comprising: a **semiconductor chip** having a number of **electrode pads**; a tape carrier comprising, a number of inner leads, where at least one of the number of inner leads is directly bonded to one of the number of

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09/26/2002 09/939,457

electrode pads, a support **film** of first thickness formed on an upper surface of the inner leads, and having an upper surface, outer lateral surface, and an inner lateral surface proximate the **semiconductor chip**, and, a number of outer leads electrically and respectively **connected** to the inner leads; and, moulding cpd. encapsulating, the number of inner leads, at least top and side surfaces of the **semiconductor chip**, and at least the inner lateral surface of the support film, and being formed to a thickness equal to the first thickness.

Dwg.9/10/1

0

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59/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009990688

WPI Acc No: 1994-258399/199432

XRFX Acc No: N94-203821

Lead frame for **semiconductor chips** - uses CCB bump to
carry out face-down mounting of chip carrier onto package substrate

Patent Assignee: SHINKO DENKI KOGYO KK (SHIA)

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 6188351	A	19940708	JP 92354569	A	19921216	199432 B
JP 3241471	B2	20011225	JP 92354569	A	19921216	200203

Priority Applications (No Type Date): JP 92354569 A 19921216

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 6188351	A	5	H01L-023/50	
JP 3241471	B2	5	H01L-023/50	Previous Publ. patent JP 6188351

Abstract (Basic): JP 6188351 A

The **semiconductor** mfg. method **connects** the **semiconductor chip** to the main, and back faces of a package substrate furnished with internal wiring. This is formed on the chip carrier by face down mounting through controlled collapse bonding (CCB) bump. The **semiconductor** IC device consists of bonding wire (16) that **connects** the CCB bump of a chip to the CCB **bump electrode**. A cap provides an air-tight sealing of the **semiconductor chip**.

A wire bonding **electrode** is formed on the upper surface of the **semiconductor chip**. This provides wiring restoration, logical restoration and serves as an object for **connection** to redundant circuits.

ADVANTAGE - Raises reliability of redundant circuit **connection** part. Simplifies design and manufacture processes, improves life-time of wiring.

Dwg.1/10

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59/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007752146

WPI Acc No: 1989-017258/198903

XRFX Acc No: N89-013303

Tape carrier for **semiconductor chips** - has **conductor**
pattern surrounding second pattern which provides leads for
connection to chip mounted in respective aperture

Patent Assignee: SHARP KK (SHAF)

Inventor: CHIKAWA Y; TAJIMA N; TSUDA T

Number of Countries: 006 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 299768	A	19890118	EP 88306454	A	19880714	198903 B
US 4949155	A	19900814	US 88219218	A	19880714	199035

Priority Applications (No Type Date): JP 87U107993 U 19870714

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 299768	A	E	10		

Designated States (Regional): CH DE FR LI NL

Abstract (Basic): EP 299768 A

The tape carrier (1) is an insulating polyimide, polyester, or glass **epoxy resin, film** of about twenty to forty metres length, 35-70 mm wide and 50-125 microns in thickness. Apertures (2) are formed in a row extending centrally and longitudinally of the tape. A respective **conductor** pattern (3) is formed around each hole by laminating a copper film on the carrier and etching it to form the pattern which has eight leads extending to the edges of the aperture.

A **semiconductor chip** (4) placed in each aperture has **electrode bumps** which are aligned with the lead ends extending to the edges of the aperture and joined to them by eutectic soldering. The copper film is etched again to form a second respective **conductor** pattern (5) forming an enclosing rail on every side of the respective first pattern. A **conductor** (6) **interconnects** respective ones of the first and second patterns.

ADVANTAGE - Chips are prevented from being damaged by electrostatic discharges and can be tested electrically whilst they are still on carrier tape

Abstract (Equivalent): US 4949155 A

The tape carrier for **semiconductor chips** has several **conductor** patterns longitudinally formed on an insulating tape and spaced from each other. Each of the patterns has a lead **connected** with a substrate **electrode** of a **semiconductor chip** and second leads **connected** with the other **electrodes** of the chip. A second stripe shaped **conductor** pattern is disposed near each of the first **conductor** patterns on the insulating tape.

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A third **conductor** pattern formed on the insulating tape has **conductors** electrically **connecting** the first lead with the second **conductor** pattern. The second **conductor** pattern is **connected** with the substrate **electrode** through the third **conductor** pattern, thereby lowering the electrostatic potential of the tape carrier. Each of these second leads is separate from any other lead and **conductor** pattern, enabling individual testing of **semiconductor chips** mounted on the tape carrier.

ADVANTAGE - Can be tested without being detached from carrier. (9pp

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59/3,AB/17 (Item 1 from file: 347)
DIALOG(R) File 347:JAPIO
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05281424

DEVICE AND METHOD FOR REMOVING **SEMICONDUCTOR**

PUB. NO.: 08-236924 [JP 8236924 A]
PUBLISHED: September 13, 1996 (19960913)
INVENTOR(s): HATSUDA TOSHIO
KOUNO MASAYA
HAYASHIDA TETSUYA
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 07-039698 [JP 9539698]
FILED: February 28, 1995 (19950228)

ABSTRACT

PURPOSE: To remove free-chip type large **semiconductors** carrying bumps on their entire surfaces or the packages of the **semiconductors** by cutting off the bumps by fusion by conducting a platy exothermic resistor, the diameter or thickness of which is made smaller than the height of the bumps.

CONSTITUTION: **Semiconductor chips** or **semiconductor** packages 1 are connected to a substrate 2 through connecting bumps 3 of solder balls, etc. An exothermic resistor 4, the diameter or thickness of which is made smaller than the height of the bumps 3, is fixed to a holder electrode 5 with exothermic resistor fixing screws 6. A holder 7 holds the electrode 5 and holds and insulates the conductor connecting the electrode 5 to a power source. The holder 7 is attached to an arm 51 connected to an XYZ stage 52, moved to the position of a **semiconductor** 1, etc., to be mounted by means of the stage 52 and, at the same time, adjusts the height of the resistor 4 so that the resistor 4 can get in between the **semiconductor** 1, etc., and the substrate 2. The resistor 4 is moved to cut off the connecting bumps 3 by fusion.

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59/3,AB/18 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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04952760

SEMICONDUCTOR PACKAGE AND ITS MANUFACTURE

PUB. NO.: 07-245360 [JP 7245360 A]
PUBLISHED: September 19, 1995 (19950919)
INVENTOR(s): IWASAKI HIROSHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 06-032296 [JP 9432296]
FILED: March 02, 1994 (19940302)

ABSTRACT

PURPOSE: To provide a **semiconductor** package wherein **cost reduction** is possible and high reliability is ensured, and a manufacturing method of the package with high yield.

CONSTITUTION: In a resin based substrate 7, a wiring circuit containing **connection** pads is formed on a main surface, and flat terminals 9 for outer **connection** arranged in a lattice type at specified pitches are led out and exposed on the other surface, via through holes 10. **Electrode** terminal parts (gold **bumps**) of a **semiconductor chip** 8 are aligned and arranged on the main surface, so as to correspond with the **connection** pads. The surface of the substrate 7 and the part of the **semiconductor chip** 8 to be **connected** are mutually pressed, fixed and **connected**, thereby assembling a **semiconductor** package. In this state, silver paste is thermoset and bonded, so that the chip is fixed on the substrate, and electric **connection** is also attained. The gap between the upper surface of the substrate 7 and the lower surface of the **semiconductor chip** 8 is filled with sealing resin and it is cured. Thereby a **semiconductor** package is completed.

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61/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014646569

WPI Acc No: 2002-467273/200250

XRPX Acc No: N02-368420

Semiconductor integrated circuit device manufacture for tape carrier package, involves packing resin between **semiconductor chip** base, support film and dam portion by discharging under-filling resin from the chip

Patent Assignee: HITACHI LTD (HITA); HITACHI TOKYO ELECTRONICS CO (HITN)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2002118127	A	20020419	JP 2000307445	A	20001006	200250 B

Priority Applications (No Type Date): JP 2000307445 A 20001006

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002118127	A		10	H01L-021/56	

Abstract (Basic): JP 2002118127 A

Abstract (Basic):

NOVELTY - An inner lead (2), a soldering resist and a dam portion (4) are sequentially formed on the periphery of support film (1a) of a tape (1). A **semiconductor chip** (5) is mounted on chip mounting area of the tape with its **bump electrode** (5a) positioned on the inner lead. A resin is provided between the chip base, support film and dam portion, by discharging under-filling resin (6) from mounting side of the chip.

USE - For manufacturing **semiconductor** integrated circuit device e.g. tape carrier package (TCP).

ADVANTAGE - Since the dam portion is formed on tape by soldering resist, the flow rate of resin is increased and wrap-round lack of resin at **semiconductor chip** mounting surface is prevented, thus the curvature of inner lead is prevented by packing the resin from mounting side of **semiconductor chip**.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view explaining manufacturing method of **semiconductor** integrated circuit device.

Tape (1)
Support film (1a)
Inner lead (2)
Dam portion (4)
Semiconductor chip (5)
Bump electrode (5a)
Under-filling resin (6)
pp; 10 DwgNo 4/7

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61/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014560925

WPI Acc No: 2002-381628/200241

Related WPI Acc No: 2002-235478; 2002-478453

XRAM Acc No: C02-107582

XRFX Acc No: N02-298637

Fabrication of **semiconductor** device assembly comprises attaching
stabilizing plate to substrate adjacent ball grid array structure

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: GOOCH S; WENSEL R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020019080	A1	20020214	US 99251252	A	19990216	200241 B
			US 2001954552	A	20010917	

Priority Applications (No Type Date): US 99251252 A 19990216; US 2001954552
A 20010917

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020019080	A1	10	H01L-021/44		Div ex application US 99251252 Div ex patent US 6291899

Abstract (Basic): US 20020019080 A1

Abstract (Basic):

NOVELTY - A **semiconductor** device assembly is fabricated by:

- (i) securing a **semiconductor chip** to a substrate surface;
- (ii) coupling a ball grid array (BGA) structure to an opposing substrate surface;
- (iii) attaching a stabilizing plate to the substrate adjacent the BGA structure; and
- (iv) encapsulating the chip and a substrate portion adjacent the chip

USE - For fabricating a **semiconductor** device (preferably BGA) assembly.

ADVANTAGE - The use of stabilizing plate increases the reliability and manufacturability of the BGA assembly, and provides a **cost** -efficient and effective **reduction** of assembly warpage.

DESCRIPTION OF DRAWING(S) - The figure shows steps in fabricating a BGA assembly.

pp; 10 DwgNo 5/5

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61/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014526687

WPI Acc No: 2002-347390/200238

XRFX Acc No: N02-273849

Semiconductor device e.g. flip-chip includes **bump electrode** which is exposed from insulating resin covering upper and lower surfaces of **semiconductor chip**

Patent Assignee: SANYO ELECTRIC CO LTD (SAOL)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2002076181	A	20020315	JP 2000258826	A	20000829	200238 B

Priority Applications (No Type Date): JP 2000258826 A 20000829

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2002076181	A	5	H01L-023/12	

Abstract (Basic): JP 2002076181 A

Abstract (Basic):

NOVELTY - The upper and lower surfaces of a **semiconductor chip** are covered by an insulating resin (4). A **bump electrode** (3) is exposed from the insulating resin.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for **semiconductor** device manufacturing method.

USE - **Semiconductor** device e.g. flip-chip mounted on circuit board.

ADVANTAGE - Reliable mounting operation of **semiconductor** device is performed, as high load **carrying** capacity of **semiconductor** device is achieved at the time of mounting **semiconductor** device in circuit board.

DESCRIPTION OF DRAWING(S) - The figure explains the **semiconductor** device manufacturing method. (Drawing includes non-English language text).

Bump electrode (3)

Insulating resin (4)

pp; 5 DwgNo 3/7

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61/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014084877

WPI Acc No: 2001-569091/200164

XRFX Acc No: N01-424110

Flip-**chip** mounting method of **semiconductor** device, involves forming two **bumps** on **electrodes** in either sides of one surface of **semiconductor** device and one **bump** on **electrode** in center of substrate

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001237270	A	20010831	JP 200044782	A	20000222	200164 B

Priority Applications (No Type Date): JP 200044782 A 20000222

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001237270	A		6 H01L-021/60	

Abstract (Basic): JP 2001237270 A

Abstract (Basic):

NOVELTY - Bumps (1a,1b) are formed on **electrodes** (2a) in either sides of **semiconductor** device (3), and **electrode** (9b) in center of substrate (9). The device is reversed, after transferring **conductive** adhesive (6) on **bumps** (1a), such that the **bumps** (1a,1b) contact **electrodes** (9a) in either sides of substrate and **electrode** (2b) in center of device. Then, ultrasonic oscillation is applied and pressed.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for mounting structure of **semiconductor** device.

USE - For flip-**chip** mounting of **semiconductor** device used for personal computer, **portable** terminal, etc., onto circuit substrate.

ADVANTAGE - Damage to mounting face of **semiconductor** device, is prevented, by securing joining reliability of **semiconductor** device and substrate.

DESCRIPTION OF DRAWING(S) - The figure shows the mounting method of **semiconductor** device. (Drawing includes non-English language text).

Bumps (1a,1b)
Electrodes (2a,2b,9a,9b)
Semiconductor device (3)
Conductive adhesive (6)
Substrate (9)
Sealing agent (10)
pp; 6 DwgNo 1/3

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61/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013076864

WPI Acc No: 2000-248736/200022

XRAM Acc No: C00-075416

XRPX Acc No: N00-186301

Resin sealing method for performing face down mounting of
semiconductor chip in **semiconductor** package - involves
supplying resin continuously using nozzle, to interstice and carrier

Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11354552	A	19991224	JP 98164926	A	19980612	200022 B

Priority Applications (No Type Date): JP 98164926 A 19980612

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11354552	A		7	H01L-021/56	

Abstract (Basic): JP 11354552 A

NOVELTY - Resin is supplied continuously using nozzle (9) to
interstice (S) and carrier, such that mounting of **semiconductor**
chip (4) via **bump electrode** at carrier is enabled.

USE - For sealing resin, and employed in face down mounting of
semiconductor chip in **semiconductor** package.

ADVANTAGE - Since continuous supply of resin is performed, inferior
sealing is eliminated. Influence by residual resin is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of
manufacturing method of **semiconductor** package. (4)

Semiconductor chip; (9) Nozzle; (S) Interstice.

Dwg.2/8

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09/26/2002 09/939,457

61/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012994532

WPI Acc No: 2000-166384/200015

XRAM Acc No: C00-052049

XRPX Acc No: N00-124879

Semiconductor chip processing system used in **portable**
information **apparatus** - forms **bump electrodes** in chip
area in wafer separated by partition lines and piers of photoresist
film, such that sealing **resin layer** is formed over

bump electrodes and removes photoresist **layer**

Patent Assignee: CASIO COMPUTER CO LTD (CASK)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000021823	A	20000121	JP 98195162	A	1998062	200015 B

Priority Applications (No Type Date): JP 98195162 A 19980626

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000021823	A		8	H01L-021/301	

Abstract (Basic): JP 2000021823 A

NOVELTY - Along the predetermined partition lines (12) separating chips (18) on wafer (11), photoresist film piers (15A) are formed. **Bump electrodes** (14) are formed with each chip area between piers. Sealing **resin layer** (17) is formed over the **bump electrodes**, and is separated by piers. Photoresist film is removed and chips are cut across partition lines using dicing blade. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **semiconductor chip** processing method.

USE - For flip-chip mounting of **chips** in **semiconductor** LSI used for **portable** information **apparatus**.

ADVANTAGE - Prevents debonding of sealing resin during cutting, because of gaps along partition lines in the sealing **resin layer**. DESCRIPTION OF DRAWING(S) - The figure shows process sectional view of **semiconductor chip**. (11) Wafer; (12) Partition line; (14) **Bump electrode**; (15A) Photoresist film piers; (17) Sealing **resin layer**; (18) Chip.

Dwg.4/10

JP 2000021823 A

NOVELTY - Along the predetermined partition lines (12) separating chips (18) on wafer (11), photoresist film piers (15A) are formed. **Bump electrodes** (14) are formed with each chip area between piers. Sealing **resin layer** (17) is formed over the **bump electrodes**, and is separated by piers. Photoresist film is removed and chips are cut across partition lines using dicing blade. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **semiconductor chip** processing method.

USE - For flip-chip mounting of **chips** in **semiconductor**

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/26/2002 09/939,457

LSI used for **portable** information **apparatus**.

ADVANTAGE - Prevents debonding of sealing resin during cutting, because of gaps along partition lines in the sealing **resin layer**. DESCRIPTION OF DRAWING(S) - The figure shows process sectional view of **semiconductor chip**. (11) Wafer; (12) Partition line; (14) **Bump electrode**; (15A) Photoresist **film** piers; (17) Sealing **resin layer**; (18) Chip.

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09/26/2002 09/939,457

61/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011637015

WPI Acc No: 1998-053923/199806

XRPX Acc No: N98-042640

Chip size **semiconductor** component - has **conductive** wire
inner ends bonded to multiple chip beads.

Patent Assignee: LG SEMICON CO LTD (GLDS); HYUNDAI MICROELECTRONICS CO
LTD (HYUN-N)

Inventor: CHA K B; YOU J H; CHA K; YU J; CHA G B; YOO J H

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19723203	A1	19980102	DE 1023203	A	19970603	199806 B
JP 10065054	A	19980306	JP 97147350	A	19970605	199820
KR 98006178	A	19980330	KR 9622507	A	19960620	199904
US 5977643	A	19991102	US 97877566	A	19970617	199953
KR 186333	B1	19990320	KR 9622507	A	19960620	200043
CN 1174403	A	19980225	CN 97103780	A	19970410	200171

Priority Applications (No Type Date): KR 9622507 A 19960620

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19723203	A1	13		H01L-023/50	
JP 10065054	A	7		H01L-023/12	
KR 98006178	A			H01L-023/28	
US 5977643	A			H01L-023/48	
KR 186333	B1			H01L-023/28	
CN 1174403	A			H01L-021/50	

Abstract (Basic): DE 19723203 A

The **semiconductor chip** (21) carries several beads (22) bonded to the inner ends of the **conductive** wires (16), in a vertical manner. The entire chip is embedded in synthetic resin (23) such that the outer ends of the **conductive** wires **protrude** outwards.

Preferably the inner end of the bonded wires, in contact with the chip beads, are shaped as irregular, oval; bonding spheres (25). Typically the outer ends of the **protruding conductive** vires are bent, directed against the middle of the chip, such as to form L-shaped external **conductors**.

USE - For advanced type integrated **semiconductor** devices.

ADVANTAGE - Provides **minimum dimensions** of **semiconductor** component, with shortest possible electric signal transmission path.

Dwg.5/11

09/26/2002 09/939,457

61/3,AB/9 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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05637227

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 09-252027 [JP 9252027 A]
PUBLISHED: September 22, 1997 (19970922)
INVENTOR(s): TAKAHASHI HIROYUKI
ARAI TAKESHI
SUWA MOTOHIRO
KAMATA CHIYOSHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 08-058061 [JP 9658061]
FILED: March 14, 1996 (19960314)

ABSTRACT

PROBLEM TO BE SOLVED: To make it possible to mount a chip on a wiring substrate at **lower cost** and in a smaller area, and to repair and/or remount it easily when failed, in a chip size package with its area being the same as **semiconductor chip**.

SOLUTION: This flip **chip semiconductor** integrated circuit device is mounted on a wiring substrate 4 by the face down bonding and constructed by a **semiconductor chip 1** with its predetermined integrated circuit formed on its main surface, a plural **bump electrode 2** formed on a scribe line on the main surface of the **semiconductor chip 1**, and a sealing resin 3 sealing a main surface of the **semiconductor chip 1** having these **bump electrodes 2**. The surfaced of the **bump electrode 2** and the sealing resin 3 are formed almost on the same plane, and the side of **bump electrode 2** is exposed, and the side of **semiconductor chip 1** and the side of **bump electrode 2** or the side of the sealing resin 3 are formed almost on the same plane.

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65/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013612839

WPI Acc No: 2001-097047/200111

XRPX Acc No: N01-073873

Manufacture of **semiconductor** device e.g. LSI, involves connecting
bump electrode on chip **electrode** pad, to
electrode pad on substrate by applying weight on chip for
carrying out reflow process and melting bump

Patent Assignee: HITACHI LTD (HITA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000332052	A	20001130	JP 99137057	A	19990518	200111 B

Priority Applications (No Type Date): JP 99137057 A 19990518

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000332052	A	7	H01L-021/60	

Abstract (Basic): JP 2000332052 A

Abstract (Basic):

NOVELTY - Several **electrode** pads (2) are provided to surface
of **semiconductor chip** (1). On the **electrode** pads,
bump electrode (3) is formed. Another **electrode** pad
is joined to substrate (4) with flux (5). By applying weight (7) on
semiconductor chip, reflow process is carried out and
melting connection between **bump electrode** and
electrode pad joined to substrate, is performed.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for
semiconductor device.

USE - For manufacturing **semiconductor** device e.g. large scale
integrated circuit (LSI) package.

ADVANTAGE - Connection reliability of **bump electrode** is
improved since influence of variations in connected regions is
minimized by weight.

DESCRIPTION OF DRAWING(S) - The figure shows principal part
sectional view explaining manufacturing method of **semiconductor**
device.

Semiconductor chip (1)

Electrode pads (2)

Bump (3)

Substrate (4)

Flux (5)

Weight (7)

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65/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011865425

WPI Acc No: 1998-282335/199825

XRFX Acc No: N98-222869

Semiconductor IC device for **portable** telephone, hand-held PC
- has solder bump connected to bump land of wiring through opening of
solder resist on wiring board and reinforcement frame which is arranged
on back side of wiring board

Patent Assignee: HITACHI LTD (HITA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10098073	A	19980414	JP 97166193	A	19970623	199825 B

Priority Applications (No Type Date): JP 96198920 A 19960729

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 10098073	A	20	H01L-021/60	

Abstract (Basic): JP 10098073 A

The device includes a **semiconductor chip** (1) provided with multiple bonding pads (7) at its periphery. An inner lead (11) of a wiring (10) formed on a flexible wiring board (2) is connected to the bonding pad.

A solder bump (4) is connected to a bump land (12) of the wiring, through an opening of a solder resist (3) formed on the wiring board. A reinforcement frame (5) is arranged on back side of the wiring board.

ADVANTAGE - Attains **small**, light **weight** and thin shaped **semiconductor chip**. Improves flat package property and heat dissipation property. Attains narrow pitching of **bump electrode**.

Dwg.2/27

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65/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010655994

WPI Acc No: 1996-152947/199616

XRPX Acc No: N96-128479

Semiconductor integrated circuit e.g. ball grid array mounted on film carrier tape - has base film with two holes and metal foil wiring layer connected to **semiconductor** IC **chip electrode** with **bump** on base film land smaller than through hole and contacting front and back of land surfaces

Patent Assignee: NEC CORP (NIDE)

Inventor: YAMASHITA C

Number of Countries: 006 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 702404	A2	19960320	EP 95306473	A	19950914	199616 B
JP 8088245	A	19960402	JP 94244922	A	19940914	199623
US 5668405	A	19970916	US 95528244	A	19950914	199743
EP 702404	A3	19971105	EP 95306473	A	19950914	199814
EP 702404	B1	20020306	EP 95306473	A	19950914	200219
DE 69525697	E	20020411	DE 625697	A	19950914	200232
			EP 95306473	A	19950914	

Priority Applications (No Type Date): JP 94244922 A 19940914

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 702404	A2	E	13	H01L-023/31	
Designated States (Regional): DE FR GB IT					
JP 8088245	A		8	H01L-021/60	
US 5668405	A		11	H01L-023/485	
EP 702404	A3			H01L-023/31	
EP 702404	B1	E		H01L-023/31	
Designated States (Regional): DE FR GB IT					
DE 69525697	E			H01L-023/31	Based on patent EP 702404

Abstract (Basic): EP 702404 A

The device includes a film carrier tape comprising a base film (2) with a device hole and a through hole (2a) and a metal foil wiring layer (3). One end of the wiring layer extends into the device hole forming an inner lead, the other end extends into the through hole forming a land with a front and back surface.

A **semiconductor** integrated circuit **chip** (1) includes an **electrode** (1a) connected to the inner lead of the wiring layer. A **conductive bump** (6) is formed on the land on the back surface of the base film. The land is smaller than the through hole, and the bump material contacts the front and back land surfaces.

USE/ADVANTAGE - For land grid array packages. Electrical characteristics of device are easily checked after mounting. State of bump and land junction is easily checked after mounting. Has excellent workability.

Dwg.3A/7

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/26/2002 09/939,457

Abstract (Equivalent): US 5668405 A

A **semiconductor** device, comprising:

a film carrier tape comprising a base film in which a device hole and through-hole are formed and a metal-foil wiring layer formed on said base film, wherein said metal-foil wiring layer includes one coplanar end extending into said device hole to form an inner lead and the other coplanar end extending onto said through-hole to form a land;

a **semiconductor** integrated circuit **chip** which is provided with an **electrode** which is connected with said inner lead of said metal-foil wiring layer;

sealing resin for protecting said **semiconductor** integrated circuit **chip**; and

a bump which is formed on said land and is formed on a front or back surface of said base film, said bump being made of a **conductor** material;

wherein an aperture with **dimensions smaller** than said through-hole is formed in the center of said land of said metal-foil wiring layer, whereby the material of the bump contacts both the front and back surfaces of the land.

Dwg.3A/7

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69/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013470024

WPI Acc No: 2000-641967/200062

XRPX Acc No: N00-476095

Semiconductor device such as ball grid array has **electrode**
for external connection that is connected to track by forming
through-hole on carrier, opposing the chip

Patent Assignee: SONY CORP (SONY)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000243872	A	20000908	JP 9942767	A	19990222	200062 B

Priority Applications (No Type Date): JP 9942767 A 19990222

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000243872	A		12 H01L-023/12	

Abstract (Basic): JP 2000243872 A

Abstract (Basic):

NOVELTY - A flat insulating carrier is prevented, so that one surface and preset space of **semiconductor chip** opposes each other. A track whose one end positioned at through-hole, is connected to projection **electrode protruding** from carrier. An **electrode** for external connection is connected to track by forming through-hole on carrier, opposing the chip.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **semiconductor** device manufacturing method.

USE - For e.g. ball grid array (BGA) and chip size package (CSP).

ADVANTAGE - Since through-hole is passed through and direct track absorbs it, melting joining of solder ball is performed easily, thereby transfer processing of former solder ball is unnecessary. Prevents drop-off solder ball during transfer. Since external connection **electrode** is reliably formed on desired position, jig usage is eliminated, thereby manufacturing **cost reduction** and productivity of **semiconductor** device is increased.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional chart of **semiconductor** device.

pp; 12 DwgNo 1/11

09/26/2002 09/939,457

69/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013262802

WPI Acc No: 2000-434707/200038

XRAM Acc No: C00-132450

XRPX Acc No: N00-324747

Semiconductor package manufacturing method involves mounting
semiconductor device on carrier substrate **electrode** and
sealing gap between them using sealing resin

Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000150555	A	20000530	JP 98318531	A	19981110	200038 B

Priority Applications (No Type Date): JP 98318531 A 19981110

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000150555	A		6	H01L-021/60	

Abstract (Basic): JP 2000150555 A

Abstract (Basic):

NOVELTY - A **bump** (3) on **electrode** (2) of
semiconductor device (1) is made to contact electroconductive
glue film (5) to form electroconductive glue (6) on bump. The device is
then placed over carrier substrate (7) with glue between **bump** and
substrate surface **electrode** (8). Gap between **semiconductor**
device and **electrode** (8) is sealed using sealing resin (10).
Thickness of the glue (6) increases with passage of time.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for
semiconductor package manufacturing apparatus.

USE - For manufacture of **semiconductor** package e.g.
chip size package using flip chip connection technique.

ADVANTAGE - Since the thickness of the glue increases with the
passage of time, the reduction in amount of glue transfer is prevented.
As the transfer of the electroconductive glue is stabilized,
reduction of **cost** of materials and **reduction** of work
process can be achieved and reliability of product can be raised.

DESCRIPTION OF DRAWING(S) - The figure shows the process sectional
view of manufacturing method of **semiconductor** package.

Semiconductor device (1)

Electrode (2)

Bump (3)

Electroconductive glue film (5)

Electroconductive glue (6)

Carrier substrate (7)

Surface **electrode** (8)

Sealing resin (10)

pp; 6 DwgNo 1/6

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

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72/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012739726

WPI Acc No: 1999-545843/199946

XRPX Acc No: N99-405013

Bare chip manufacturing method for testing IC device - involves
positioning **semiconductor chip** using guide ring of bare chip
carrier by adjusting each **bump electrode** to contact inner
leads of wiring board

Patent Assignee: HITACHI LTD (HITA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11237435	A	19990831	JP 9857478	A	19980223	199946 B

Priority Applications (No Type Date): JP 9857478 A 19980223

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11237435	A		8	G01R-031/26	

Abstract (Basic): JP 11237435 A

NOVELTY - Several **bump electrodes** are **protruded**
from a bare **chip**. The **semiconductor chip** is
positioned by a guide ring (30) of a bare chip carrier (10). Each bump
is adjusted and contacted by each inner lead (25) formed on a wiring
board (20) of the bare chip carrier. Outer lead (26) is connected to
the inner leads and external terminal of a tester. DETAILED DESCRIPTION
- An INDEPENDENT CLAIM is also included for the bare chip carrier.

USE - For testing IC device.

ADVANTAGE - Even a **semiconductor chip** with a high bump
density can be correctly aligned with inner lead of wiring board using
guide ring and therefore electric connection is appropriately
securable. DESCRIPTION OF DRAWING(S) - The figure shows the top view
and front sectional view of the bare chip carrier. (10) Bare chip
carrier; (20) Wiring board; (25) Inner lead; (26) Outer lead; (30)
Guide ring.

Dwg.1/8

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72/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010902404

WPI Acc No: 1996-399355/199640

XRAM Acc No: C96-125517

XRFX Acc No: N96-336634

Mfg. **semiconductor** device with projected type **bump**
electrodes e.g. for npn transistor - involves forming composite
bump made of metal film with large coefficient of expansion which covers
convex shaped object made of polyimide resin

Patent Assignee: FUJI ELECTRIC CO LTD (FJIE)

Inventor: AMANO A

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8195397	A	19960730	JP 956098	A	19950119	199640 B
SE 9600180	A	19960720	SE 96180	A	19960118	199642

Priority Applications (No Type Date): JP 956098 A 19950119

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8195397	A		8	H01L-021/321	
SE 9600180	A			H01L-021/60	

Abstract (Basic): JP 8195397 A

The method involves usage of a convex shaped object (18) which forms the **electrode** part on the main surface of a **semiconductor chip** (1). The convex shaped object made of polyimide resin consists of small modulus of elasticity. A composite bump (20) which covers object is provided. The bump consists of a metal film like Al/Si alloy film with large coefficient of expansion.

A **protruding electrode** with a large current **carrying** capacity is provided with the composite bump. Pressure application contact of the **electrode** board holding the **electrodes** is carried out on a composite bump.

ADVANTAGE - Obtains reliable and uniform bump. Eliminates need for wet electrolytic plating.

Dwg.1/14

09/26/2002 09/939,457

72/3,AB/3 (Item 3 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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001520232

WPI Acc No: 1976-J3167X/197638

SCR with cylindrical **electrode** on **conductive** substrate - has
semiconductor chip inside **electrode** on substrate

Patent Assignee: BENDIX CORP (BEND)

Number of Countries: 003 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 2604722	A	19760909				197638 B
US 4063348	A	19771220				197801
US 4068368	A	19780117				197805
GB 1505457	A	19780330				197813

Priority Applications (No Type Date): US 75621917 A 19751014; US 75553778 A
19750227

Abstract (Basic): DE 2604722 A

The controlled silicon rectifier has a base-plate (7) of **conductive** material, to which is connected a cylindrical **electrode** (11, 31). Inside this **electrode** and on the base-plate is mounted a **semiconductor chip** (14), while a spring loaded **electrode** (17), coaxial with the cylindrical **electrode**, abuts the **semiconductor chip** and presses it in positive connection with the base-plate. Preferably the cylindrical **electrode** is secured to a metal plate with an aperture (29) and insulated from the same. This metal plate (27) carries the spring loaded **electrode** (17) which **protrudes** through the aperture (29). The cylindrical **electrode** may consist of two sections, the lower one connected to the base plate and **carrying** the upper annular section.

09/26/2002 09/939,457

72/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07124278

SEMICONDUCTOR DEVICE

PUB. NO.: 2001-351946 [JP 2001351946 A]
PUBLISHED: December 21, 2001 (20011221)
INVENTOR(s): HAMADA SHIGERU
KAMIGAI YASUMI
TANI SHUICHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 2000-167737 [JP 2000167737]
FILED: June 05, 2000 (20000605)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a highly reliable **semiconductor** device, in which the occurrence of disconnections in the junction interfaces between junctions and IC **electrode** sections and between the junctions and substrate **electrode** sections is reduced by reinforcing the jointing strengths between the junctions and electrode sections in the interfaces.

SOLUTION: This **semiconductor** device is provided with a **semiconductor** IC chip section carrying a plurality of IC **electrode** sections on one surface, a mounting substrate section carrying a plurality of substrate **electrode** sections on one surface, and a plurality of junctions which join the IC **electrode** sections to their corresponding substrate **electrode** sections, the IC **electrode** sections have first projecting sections, which are fixed to the **electrode** sections and protruded into the junctions and the substrate **electrode** sections have second projecting sections, which are fixed to the **electrode** sections and protruded into the junctions so that the reliability of the **semiconductor** device is improved.

09/26/2002 09/939,457

75/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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05045517 JICST ACCESSION NUMBER: 02A0076644 FILE SEGMENT: JICST-E

Development of Advanced 3-Dimensional Chip Stacking LSI Technology.

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(1) Assoc. Super-Advanced Electronics Technol., JPN

Handotai, Shuseki Kairo Gijutsu Shinpojiumu Koen Ronbunshu(Proceedings of
the Symposium on Semiconductors and Integrated Circuits Technology),
2001, VOL.61st, PAGE.6-10,12, FIG.14, REF.22

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ARTICLE TYPE: Commentary

MEDIA TYPE: Printed Publication

ABSTRACT: We are focusing on three fields: (1) 3-dimensional (3-D) LSI chip integration technology, (2) Opto-electronic Packaging Technology and (3) Optimum circuit design technology. In this paper, we describe the 3-D LSI chip integration technology using chip stacking (3-D chip stacking LSI technology). Our development of the 3-D chip stacking LSI technology is divided into (1) wafer process, (2) wafer backside process, and (3) chip stacking process. The wafer process is further processed into the device-ready wafer which is ended the usual LSI process. At the process, Cu **electrodes** are embedded into the Si substrate with the process similar to a dual damascene Cu process, and then bumps are made on the Cu **electrodes**. The **electrode's** size is 10 .MU.m in square and 70 .MU.m in depth and they have formed in a line in the 20 .MU.m pitch. We just began to **carry** out this process on the wafer with real 0.25 .MU.m ASIC devices. The wafer backside process is the simultaneous grinding of Si and embedded Cu from the back side of the wafer, grinding damage removal and Cu plug formation by dry etching to Si-substrate, **bumping** on Cu **electrodes** of the **back** side, and handling of thinned wafer. At this process, the embedded Cu **electrodes** become through-**electrodes**. This process is followed Cu contamination on Si. We evaluate not only treatments to remove the Cu contamination, but also another process flow to form the through-**electrodes** like not to expose the Cu and Si surface simultaneously. Chip stacking technology was focused on high-accuracy bonding, encapsulation and reliability. The positioning accuracy corresponding to the 20 .MU.m-pitch-Bumps is acquired. Various material and technique are evaluated about bump bonding. From now on, the multi-chip stacking in a real device with the through-**electrodes** will be checked. (author abst.)

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75/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013882198

WPI Acc No: 2001-366410/200138
Related WPI Acc No: 1998-437666
XRAM Acc No: C01-112259
XRPX Acc No: N01-267287

Protecting **semiconductor** circuit from electrostatic discharge,
includes forming bonding points and **conductive** path on **back**
side of substrate, and forming contact points on front side of substrate
Patent Assignee: TRANSACTION TECHNOLOGY INC (TRAN-N)
Inventor: KAWAN J C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6235553	B1	20010522	US 97784262	A	19970115	200138 B
			US 98190265	A	19981112	

Priority Applications (No Type Date): US 98190265 A 19981112; US 97784262 A
19970115

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6235553	B1	16	H01L-021/44		CIP of application US 97784262 CIP of patent US 5837153

Abstract (Basic): US 6235553 B1

Abstract (Basic):

NOVELTY - A **semiconductor chip**, which is attached to a substrate, is protected from electrostatic discharge (ESD) by forming bonding points and a **conductive** path on the **back** side of the substrate; and forming contact points on the front side of the substrate.

DETAILED DESCRIPTION - Protecting a **semiconductor chip** on a substrate from ESD, comprises (a) etching a first **conductive** material on the **back** side of the substrate to form bonding points; (b) etching a second material on the back side of the substrate to form a **conductive** path; (c) creating holes through the substrate directly above the bonding points; and (d) etching a third **conductive** material on the **front** side of the substrate to form contact points. The bonding points are coupled to the chip, and the contact points are coupled to the bonding points via the holes. The **conductive** path is coupled to a first bonding point and is laid out near a second bonding point. An INDEPENDENT CLAIM is also included for a method of discharging a smart card which contains a **semiconductor chip**, a visible portion, a non-visible portion, and a charge on the visible or non-visible portion, comprising (a) **carrying** the charge through a high impedance path to a low impedance path, and (b) **carrying** the charge through the low impedance path to a low potential.

USE - For protecting a **semiconductor** circuit from ESD.

ADVANTAGE - The inventive method does not disturb the appearance of

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the contact points whether they are shaped as logo or otherwise. It does not alter the fabrication process involved in forming the contact points, and is less costly.

pp; 16 DwgNo 0/10

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75/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012433188

WPI Acc No: 1999-239296/199920

XRAM Acc No: C99-070245

XRFX Acc No: N99-178562

Chip mounting structure in **semiconductor** device - has chip
surface electric **conduction layer** and electric
conduction shield layer connected electrically, using
bump electrode

Patent Assignee: SUMITOMO ELECTRIC IND CO (SUME)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11068029	A	19990309	JP 97219537	A	19970814	199920 B

Priority Applications (No Type Date): JP 97219537 A 19970814

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11068029	A	8	H01L-023/58	

Abstract (Basic): JP 11068029 A

NOVELTY - An electric **conduction shield layer** (16) is
formed in a substrate (2) on which a **semiconductor chip** (6)
is mounted. The chip includes a chip surface electric **conduction**
layer (12). The chip surface electric **conduction**
layer and the electric **conduction shield layer** are
connected electrically using a **bump electrode** (18).

DETAILED DESCRIPTION - A current **carrying** portion (10) connects
the chip **back side electric conduction layer** (8) and
a chip surface electric **conduction layer** (12) via
connection hole. A through-hole (26) electrically connects the
substrate **back side electric conduction layer** (24)
and the electric **conduction shield layer** (16).

USE - In **semiconductor** device.

ADVANTAGE - Cuts off the external noise from the surface by
electrically connecting the **conductive layers**.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of
cross-section line of **semiconductor** device. (2) Substrate; (6)

Semiconductor chip; (8) **Chip back side electric**
conduction layer; (10) Current **carrying** portion; (12)
Chip surface electric **conduction layer**; (16) Electric
conduction shield layer; (18) **Bump electrode**; (24)
Substrate back side electric **conduction layer**; (26)
Through-hole current **carrying** portion.

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75/3,AB/4 (Item 3 from file: 350)
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010951626

WPI Acc No: 1996-448576/199645

XRPX Acc No: N96-378146

Semiconductor package e.g. tape carrier package used as drive integrated circuit - has **semiconductor chip** positioned in hole formed at base, which is connected with inner lead of copper pattern in which support component is formed at **back** side through **bump electrode**

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8222604	A	19960830	JP 9527012	A	19950215	199645 B

Priority Applications (No Type Date): JP 9527012 A 19950215

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8222604	A		4	H01L-021/60	

Abstract (Basic): JP 8222604 A

The package has a hole (5) formed in a selected position at a base material (1). A support component (7) is formed at the back side of a copper pattern (11) extended at the hole.

The **bump electrode** (14) of a **semiconductor chip** (13) provided at the hole is connected with the copper pattern through an inner lead (10).

ADVANTAGE - Prevents bending of both inner lead and outer lead in vertical direction. Prevents short circuit caused by contacting of inner lead and **semiconductor chip**.

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75/3,AB/5 (Item 4 from file: 350)
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008317637

WPI Acc No: 1990-204638/199027

Related WPI Acc No: 1989-238323; 1989-296118; 1990-032675; 1997-308364;
1997-308390; 1998-404594; 1998-404599; 1998-419872

XRAM Acc No: C91-090405

XRPX Acc No: N91-159166

Film carrier multi-**chip semiconductor** device - bends part of
outer lead to fix to film carrier substrate back face and **conducts**
front-back conduction

Patent Assignee: HITACHI LTD (HITA); HITACHI TOBU SEMICONDUCTOR LTD
(HITA-N); HITACHI MFG CO (HITA)

Inventor: HONDA M; KANEDA A; KOMARU T; NAGAOKA K; NAKAMURA A; NISHI K;
SAKAGUCHI S; SERIZAWA K; SUGANO T; TANIMOTO M; TSUKUI S; WAKASHIMA Y;
WATANABE M; YOSHIDA T

Number of Countries: 003 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2134859	A	19900523	JP 88287658	A	19881116	199027 B
US 5028986	A	19910702	US 88288955	A	19881223	199129
US 5198888	A	19930330	US 90631154	A	19901220	199315
US 5334875	A	19940802	US 88288955	A	19881223	199430
			US 90631154	A	19901220	
			US 931649	A	19930302	
KR 9707129	B1	19970502	KR 8817489	A	19881226	199941

Priority Applications (No Type Date): JP 88287658 A 19881116; JP 87332126 A
19871228; JP 8842069 A 19880226; JP 88139304 A 19880608

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2134859	A		6		
US 5028986	A		52		patent JP 1173742 patent JP 1217933 patent JP 1309362
US 5198888	A		48	H01L-023/16	
US 5334875	A		51	H01L-023/16	Div ex application US 88288955 Div ex application US 90631154 patent JP 1173742 patent JP 1217933 patent JP 1309362 Div ex patent US 5028986 Div ex patent US 5198888

KR 9707129 B1 H01L-023/50

Abstract (Basic): JP 2134859 A

The **semiconductor** memory device comprises two
semiconductor memory **chips** which are stacked one above the
other, each chip having a number of first and second **electrodes**
on first and second principal surfaces, and two connectors, each having
a first and second **conductors** arranged on first and second

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surfaces, with first **conductors** being electrically connected to respective second **conductors**.

The first **electrodes** and the second **electrode** formed on the first memory chip are electrically connected to respective **conductors** of the first **conductors** of the first connector. The first **electrodes** and the second **electrode** formed on the second memory chip are electrically connected to respective **conductors** of the first **conductors** of the second connector. The first and second connectors are stacked one above the other, with the second **conductors** of the first connector being electrically connected to respective **conductors** of the first **conductors** of the second connector. The first **electrodes** of the first memory chip are electrically connected to respective **electrodes** of the first **electrodes** of the second memory chip via the first and second **conductors**, and the second **electrode** of the first memory chip is electrically independent of the second **electrode** of the second memory chip.

ADVANTAGE - Increased mounting density. Has memory capacity number of times as large as that of conventional device for same mounting area
Abstract (Equivalent): US 5198888 A

The **semiconductor** device is formed by stacking a number of **semiconductor chips** on the outer leads of the TABs formed by the TAB (Tape Automated Bonding) method while interposing connectors formed with wiring patterns. In the **semiconductor chips** to be stacked, specifically, the stacking is accomplished so that the terminals shared for signals may be connected through the respective wiring patterns of the connectors. The chip selecting terminals left unshared have to lead in or out the signals separately to or from the **semiconductor chips**, and only the corresponding wiring patterns of the connectors are so staggered that they may not be shorted. The signals are fed to all the common terminals of the **semiconductor chips** by a single signal feed. When a signal is fed to one of the chip selecting terminals, only one of the **semiconductor chips** can be selectively used. USE/ADVANTAGE - Increased memory capacity for same mounting area of TABs, increased mounting density, simplified fabrication. (Dwg.12/63)

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75/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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008145674

WPI Acc No: 1990-032675/199005

Related WPI Acc No: 1989-238323; 1989-296118; 1990-204638; 1997-308364;
1997-308390; 1998-404594; 1998-404599; 1998-419872

Film carrier multi-**chip semiconductor** device - bends part of
outer lead to fix to film carrier substrate back face and **conducts**
front-back conduction

Patent Assignee: HITACHI LTD (HITA); HITACHI TOBU SEMICONDUCTOR LTD
(HITA-N); HITACHI MFG CO (HITA)

Inventor: HONDA M; KANEDA A; KOMARU T; NAGAOKA K; NAKAMURA A; NISHI K;
SAKAGUCHI S; SERIZAWA K; SUGANO T; TANIMOTO M; TSUKUI S; WAKASHIMA Y;
WATANABE M; YOSHIDA T

Number of Countries: 003 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 1309362	A	19891213	JP 88139304	A	19880608	199005 B
US 5028986	A	19910702	US 88288955	A	19881223	199129
US 5198888	A	19930330	US 90631154	A	19901220	199315
US 5334875	A	19940802	US 88288955	A	19881223	199430
			US 90631154	A	19901220	
			US 931649	A	19930302	
KR 9707129	B1	19970502	KR 8817489	A	19881226	199941

Priority Applications (No Type Date): JP 88139304 A 19880608; JP 87332126 A
19871228; JP 8842069 A 19880226; JP 88287658 A 19881116

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 1309362	A		5		
US 5028986	A		52		patent JP 1173742 patent JP 1217933 patent JP 1309362
US 5198888	A		48	H01L-023/16	
US 5334875	A		51	H01L-023/16	Div ex application US 88288955 Div ex application US 90631154 patent JP 1173742 patent JP 1217933 patent JP 1309362 Div ex patent US 5028986 Div ex patent US 5198888
KR 9707129	B1			H01L-023/50	

Abstract (Basic): JP 1309362 A

The **semiconductor** memory device comprises two
semiconductor memory **chips** which are stacked one above the
other, each chip having a number of first and second **electrodes**
on first and second principal surfaces, and two connectors, each having
a first and second **conductors** arranged on first and second
surfaces, with first **conductors** being electrically connected to

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respective second **conductors**.

The first **electrodes** and the second **electrode** formed on the first memory chip are electrically connected to respective **conductors** of the first **conductors** of the first connector. The first **electrodes** and the second **electrode** formed on the second memory chip are electrically connected to respective **conductors** of the first **conductors** of the second connector. The first and second connectors are stacked one above the other, with the second **conductors** of the first connector being electrically connected to respective **conductors** of the first **conductors** of the second connector. The first **electrodes** of the first memory chip are electrically connected to respective **electrodes** of the first **electrodes** of the second memory chip via the first and second **conductors**, and the second **electrode** of the first memory chip is electrically independent of the second **electrode** of the second memory chip.

ADVANTAGE - Increased mounting density. Has memory capacity number of times as large as that of conventional device for same mounting area
Abstract (Equivalent): US 5334875 A

The **semiconductor** memory device comprises two **semiconductor** memory **chips** which are stacked one above the other, each chip having a number of first and second **electrodes** on first and second principal surfaces, and two connectors, each having a first and second **conductors** arranged on first and second surfaces, with first **conductors** being electrically connected to respective second **conductors**.

The first **electrodes** and the second **electrode** formed on the first memory chip are electrically connected to respective **conductors** of the first **conductors** of the first connector. The first **electrodes** and the second **electrode** formed on the second memory chip are electrically connected to respective **conductors** of the first **conductors** of the second connector. The first and second connectors are stacked one above the other, with the second **conductors** of the first connector being electrically connected to respective **conductors** of the first **conductors** of the second connector. The first **electrodes** of the first memory chip are electrically connected to respective **electrodes** of the first **electrodes** of the second memory chip via the first and second **conductors**, and the second **electrode** of the first memory chip is electrically independent of the second **electrode** of the second memory chip.

ADVANTAGE - Increased mounting density. Has memory capacity number of times as large as that of conventional device for same mounting area.

Dwg.12/63

US 5198888 A

The **semiconductor** device is formed by stacking a number of **semiconductor** **chips** on the outer leads of the TABs formed by the TAB (Tape Automated Bonding) method while interposing connectors formed with wiring patterns. In the **semiconductor** **chips** to be stacked, specifically, the stacking is accomplished so that the terminals shared for signals may be connected through the respective wiring patterns of the connectors. The chip selecting terminals left unshared have to lead in or out the signals separately to or from the

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semiconductor chips, and only the corresponding wiring patterns of the connectors are so staggered that they may not be shorted. The signals are fed to all the common terminals of the **semiconductor chips** by a single signal feed. When a signal is fed to one of the chip selecting terminals, only one of the **semiconductor chips** can be selectively used. USE/ADVANTAGE
- Increased memory capacity for same mounting area of TABs, increased mounting density, simplified fabrication.
Dwg.12/63

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75/3,AB/7 (Item 6 from file: 350)
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008031006

WPI Acc No: 1989-296118/198941

Related WPI Acc No: 1989-238323; 1990-032675; 1990-204638; 1997-308364;
1997-308390; 1998-404594; 1998-404599; 1998-419872

XRAM Acc No: C89-131103

XRPX Acc No: N89-225709

Film carrier multi-**chip semiconductor** device - bends part of
outer lead to fix to film carrier substrate back face and **conducts**
front-back conduction

Patent Assignee: HITACHI LTD (HITA); HITACHI TOBU SEMICONDUCTOR LTD
(HITA-N); HITACHI MFG CO (HITA)

Inventor: HONDA M; KANEDA A; KOMARU T; NAGAOKA K; NAKAMURA A; NISHI K;
SAKAGUCHI S; SERIZAWA K; SUGANO T; TANIMOTO M; TSUKUI S; WAKASHIMA Y;
WATANABE M; YOSHIDA T

Number of Countries: 003 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 1217933	A	19890831	JP 8842069	A	19880226	198941 B
US 5028986	A	19910702	US 88288955	A	19881223	199129
US 5198888	A	19930330	US 90631154	A	19901220	199315
US 5334875	A	19940802	US 88288955	A	19881223	199430
			US 90631154	A	19901220	
			US 931649	A	19930302	
KR 9707129	B1	19970502	KR 8817489	A	19881226	199941

Priority Applications (No Type Date): JP 8842069 A 19880226; JP 87332126 A
19871228; JP 88139304 A 19880608; JP 88287658 A 19881116

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5028986	A		52		patent JP 1173742 patent JP 1217933 patent JP 1309362
US 5198888	A		48	H01L-023/16	
US 5334875	A		51	H01L-023/16	Div ex application US 88288955 Div ex application US 90631154 patent JP 1173742 patent JP 1217933 patent JP 1309362 Div ex patent US 5028986 Div ex patent US 5198888
KR 9707129	B1			H01L-023/50	

Abstract (Basic): JP 1217933 A

The **semiconductor** memory device comprises two
semiconductor memory **chips** which are stacked one above the
other, each chip having a number of first and second **electrodes**
on first and second principal surfaces, and two connectors, each having
a first and second **conductors** arranged on first and second

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surfaces, with first **conductors** being electrically connected to respective second **conductors**.

The first **electrodes** and the second **electrode** formed on the first memory chip are electrically connected to respective **conductors** of the first **conductors** of the first connector. The first **electrodes** and the second **electrode** formed on the second memory chip are electrically connected to respective **conductors** of the first **conductors** of the second connector. The first and second connectors are stacked one above the other, with the second **conductors** of the first connector being electrically connected to respective **conductors** of the first **conductors** of the second connector. The first **electrodes** of the first memory chip are electrically connected to respective **electrodes** of the first **electrodes** of the second memory chip via the first and second **conductors**, and the second **electrode** of the first memory chip is electrically independent of the second **electrode** of the second memory chip.

ADVANTAGE - Increased mounting density. Has memory capacity number of times as large as that of conventional device for same mounting area.

US 5198888 A

The **semiconductor** device is formed by stacking a number of **semiconductor chips** on the outer leads of the TABs formed by the TAB (Tape Automated Bonding) method while interposing connectors formed with wiring patterns. In the **semiconductor chips** to be stacked, specifically, the stacking is accomplished so that the terminals shared for signals may be connected through the respective wiring patterns of the connectors. The chip selecting terminals left unshared have to lead in or out the signals separately to or from the **semiconductor chips**, and only the corresponding wiring patterns of the connectors are so staggered that they may not be shorted. The signals are fed to all the common terminals of the **semiconductor chips** by a single signal feed. When a signal is fed to one of the chip selecting terminals, only one of the **semiconductor chips** can be selectively used. USE/ADVANTAGE - Increased memory capacity for same mounting area of TABs, increased mounting density, simplified fabrication. (Dwg.12/63)

Abstract (Equivalent): US 5334875 A

The **semiconductor** memory device comprises two **semiconductor** memory **chips** which are stacked one above the other, each chip having a number of first and second **electrodes** on first and second principal surfaces, and two connectors, each having a first and second **conductors** arranged on first and second surfaces, with first **conductors** being electrically connected to respective second **conductors**.

The first **electrodes** and the second **electrode** formed on the first memory chip are electrically connected to respective **conductors** of the first **conductors** of the first connector. The first **electrodes** and the second **electrode** formed on the second memory chip are electrically connected to respective **conductors** of the first **conductors** of the second connector. The first and second connectors are stacked one above the other, with the second **conductors** of the first connector being electrically connected to respective **conductors** of the first **conductors**

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of the second connector. The first **electrodes** of the first memory chip are electrically connected to respective **electrodes** of the first **electrodes** of the second memory chip via the first and second **conductors**, and the second **electrode** of the first memory chip is electrically independent of the second **electrode** of the second memory chip.

ADVANTAGE - Increased mounting density. Has memory capacity number of times as large as that of conventional device for same mounting area.

Dwg.12/63

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75/3,AB/8 (Item 7 from file: 350)
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007973211

WPI Acc No: 1989-238323/198933

Related WPI Acc No: 1989-296118; 1990-032675; 1990-204638; 1997-308364;
1997-308390; 1998-404594; 1998-404599; 1998-419872

XRPX Acc No: N89-181411

Film carrier multi-**chip semiconductor** device - bends part of
outer lead to fix to film carrier substrate back face and **conducts**
front-back conduction

Patent Assignee: HITACHI DEVICE ENGINEERING LTD (HITA); HITACHI LTD (HITA
); HITACHI TOBU SEMICONDUCTOR LTD (HITA-N); HITACHI MFG CO (HITA)

Inventor: HONDA M; KANEDA A; KOMARU T; NAGAOKA K; NAKAMURA A; NISHI K;
SAKAGUCHI S; SERIZAWA K; SUGANO T; TANIMOTO M; TSUKUI S; WAKASHIMA Y;
WATANABE M; YOSHIDA T

Number of Countries: 003 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 1173742	A	19890710	JP 87332126	A	19871228	198933 B
US 5028986	A	19910702	US 88288955	A	19881223	199129
US 5198888	A	19930330	US 90631154	A	19901220	199315
US 5334875	A	19940802	US 88288955	A	19881223	199430
			US 90631154	A	19901220	
			US 931649	A	19930302	
KR 9707129	B1	19970502	KR 8817489	A	19881226	199941

Priority Applications (No Type Date): JP 87332126 A 19871228; JP 8842069 A
19880226; JP 88139304 A 19880608; JP 88287658 A 19881116

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 1173742	A		4		
US 5028986	A		52		patent JP 1173742 patent JP 1217933 patent JP 1309362
US 5198888	A		48	H01L-023/16	
US 5334875	A		51	H01L-023/16	Div ex application US 88288955 Div ex application US 90631154 patent JP 1173742 patent JP 1217933 patent JP 1309362 Div ex patent US 5028986 Div ex patent US 5198888
KR 9707129	B1			H01L-023/50	

Abstract (Basic): JP 1173742 A

The **semiconductor** memory device comprises two
semiconductor memory **chips** which are stacked one above the
other, each chip having a number of first and second **electrodes**
on first and second principal surfaces, and two connectors, each having
a first and second **conductors** arranged on first and second

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surfaces, with first **conductors** being electrically connected to respective second **conductors**.

The first **electrodes** and the second **electrode** formed on the first memory chip are electrically connected to respective **conductors** of the first **conductors** of the first connector. The first **electrodes** and the second **electrode** formed on the second memory chip are electrically connected to respective **conductors** of the first **conductors** of the second connector. The first and second connectors are stacked one above the other, with the second **conductors** of the first connector being electrically connected to respective **conductors** of the first **conductors** of the second connector. The first **electrodes** of the first memory chip are electrically connected to respective **electrodes** of the first **electrodes** of the second memory chip via the first and second **conductors**, and the second **electrode** of the first memory chip is electrically independent of the second **electrode** of the second memory chip.

ADVANTAGE - Increased mounting density. Has memory capacity number of times as large as that of conventional device for same mounting area.

US 5198888 A

The **semiconductor** device is formed by stacking a number of **semiconductor chips** on the outer leads of the TABs formed by the TAB (Tape Automated Bonding) method while interposing connectors formed with wiring patterns. In the **semiconductor chips** to be stacked, specifically, the stacking is accomplished so that the terminals shared for signals may be connected through the respective wiring patterns of the connectors. The chip selecting terminals left unshared have to lead in or out the signals separately to or from the **semiconductor chips**, and only the corresponding wiring patterns of the connectors are so staggered that they may not be shorted. The signals are fed to all the common terminals of the **semiconductor chips** by a single signal feed. When a signal is fed to one of the chip selecting terminals, only one of the **semiconductor chips** can be selectively used. USE/ADVANTAGE - Increased memory capacity for same mounting area of TABs, increased mounting density, simplified fabrication. (Dwg.12/63)

Abstract (Equivalent): US 5334875 A

The **semiconductor** memory device comprises two **semiconductor** memory **chips** which are stacked one above the other, each chip having a number of first and second **electrodes** on first and second principal surfaces, and two connectors, each having a first and second **conductors** arranged on first and second surfaces, with first **conductors** being electrically connected to respective second **conductors**.

The first **electrodes** and the second **electrode** formed on the first memory chip are electrically connected to respective **conductors** of the first **conductors** of the first connector. The first **electrodes** and the second **electrode** formed on the second memory chip are electrically connected to respective **conductors** of the first **conductors** of the second connector. The first and second connectors are stacked one above the other, with the second **conductors** of the first connector being electrically connected to respective **conductors** of the first **conductors**

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of the second connector. The first **electrodes** of the first memory chip are electrically connected to respective **electrodes** of the first **electrodes** of the second memory chip via the first and second **conductors**, and the second **electrode** of the first memory chip is electrically independent of the second **electrode** of the second memory chip.

ADVANTAGE - Increased mounting density. Has memory capacity number of times as large as that of conventional device for same mounting area.

Dwg.12/63

09/26/2002 09/939,457

26sep02 13:43:06 User267149 Session D360.1

SYSTEM:OS - DIALOG OneSearch

File 348:EUROPEAN PATENTS 1978-2002/Sep W03
(c) 2002 European Patent Office

File 349:PCT FULLTEXT 1983-2002/UB=20020912,UT=20020905
(c) 2002 WIPO/Univentio

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Set	Items	Description
S1	2182	((PORTABLE OR CARRY?????) (3N) (ELECTRONIC?????? OR NOTEBOOK? ? OR NOTE()BOOK? ? OR LAPTOP? ? OR LAP()TOP ? OR VIDEO OR CA- MERA? ? OR VIDEO()CAMERA)) /TI,AB,CM
S2	118570	((PORTABLE OR CARRY?????) /TI,AB,CM
S3	8510	((PORTABLE OR CARRY?????) (3N) APPARAT?????) /TI,AB,CM
S4	10145	((SMALL?????? OR MINIM?????? OR REDUC??????) (3N) (DIMENSION? ? OR WEIGHT????)) /TI,AB,CM
S5	2653	((REDUC?????? OR LOWER???? OR MINIM??????) (3N) COST?????) /- TI,AB,CM
S6	129779	S1:S5
S7	103524	SEMICONDUCT?????
S8	3736	(SEMICONDUCT?????? (3N) CHIP? ?) /TI,AB,CM
S9	127	(SANDWICH?????? (3N) CIRCUIT???) /TI,AB,CM
S10	3862	S8:S9
S11	198572	(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????) /TI,AB,- CM
S12	30663	((ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????) (3N) (LA- YER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER????)) /- TI,AB,CM
S13	198572	S11:S12
S14	1760	((ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????) (3N) (RE- AR OR BACK)) /TI,AB,CM
S15	595	(PROTRUD?????? (3N) (ELECTRODE? ? OR MICROELECTRODE? ? OR CO- NDUCT????)) /TI,AB,CM
S16	966	((ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????) (3N) FRO- NT) /TI,AB,CM
S17	440	(BUMP?????? (3N) (ELECTRODE? ? OR MICROELECTRODE? ? OR CONDU- CT????)) /TI,AB,CM
S18	1963	S15:S17
S19	29115	((INSULAT?????? OR DIELECTRIC???) (3N) (LAYER??? OR FILM??? - OR COAT??? OR MULTILAYER??? OR SPACER????)) /TI,AB,CM
S20	13492	(RESIN??? (N3) (LAYER????? OR FILM??? OR COAT????)) /TI,AB,CM
S21	37189	((EPOX??? OR RESIN? ? OR THERMOPLASTIC??? OR ELASTOMER?? OR RUBBER? ? OR ADHESIVE??) (N3) (LAYER??? OR FILM??? OR COAT???-)) /TI,AB,CM
S22	169357	POLYMER???? /TI,AB,CM
S23	169358	(POLYMER???? OR HOMOPOLYMER????? OR COPOLYMER????) /TI,AB,CM
S24	192067	S20:S23
S25	28150	((INTERCONNECT?????? OR CONNECT??????) (3N) (LINE? ? OR LINI- NG)) /TI,AB,CM
S26	484650	(INTERCONNECT?????? OR CONNECT??????) /TI,AB,CM
S27	12762	(PRINT?????? (3N) CIRCUIT??????) /TI,AB,CM
S28	16322	(CIRCUIT?????? (3N) BOARD??????) /TI,AB,CM
S29	1991	((WIRE?? OR WIRING) (3N) BOND??????) /TI,AB,CM
S30	19018	S27:S28
S31	484650	S25:S26
S32	332	S6 AND S10
S33	254	S32 AND S13
S34	3	S33 AND S14
S35	251	S33 NOT S34
S36	12	S35 AND S18
S37	3	S36 AND S19

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S38	9	S36 NOT S37
S39	3	S38 AND S24
S40	6	S38 NOT S39
S41	6	IDPAT (sorted in duplicate/non-duplicate order)
S42	239	S35 NOT S36
S43	0	S42 AND S14
S44	0	S42 AND S18
S45	38	S42 AND S19
S46	15	S45 AND S24
S47	13	S46 AND S31
S48	5	S47 AND S30
S49	5	IDPAT (sorted in duplicate/non-duplicate order)
S50	1	S49 AND S29
S51	4	S49 NOT S50
S52	8	S47 NOT S49
S53	8	IDPAT (sorted in duplicate/non-duplicate order)
S54	25	S45 NOT S47
S55	20	S54 AND S2
S56	0	S55 AND S14
S57	0	S55 AND S120
S58	0	S55 AND S21
S59	20	S55 AND S7
S60	20	S55 AND S8
S61	20	IDPAT (sorted in duplicate/non-duplicate order)
S62	1	S61 AND S4
S63	19	S61 NOT S62
S64	0	S63 AND S5
S65	0	S63 AND S9
S66	19	S63 AND S11
S67	0	S66 AND S15
S68	0	S66 AND S16
S69	0	S66 AND S17
S70	1	S66 AND S25
S71	18	S66 NOT S70
?		

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34/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

SEMICONDUCTOR DEVICE, METHOD OF MANUFACTURING ELECTRONIC DEVICE,
ELECTRONIC DEVICE, AND PORTABLE INFORMATION TERMINAL
HALBLEITERANORDNUNG, METHODE ZUR HERSTELLUNG EINER ELEKTRONISCHEN
SCHALTUNG, ELEKTRONISCHE SCHALTUNG, UND TRAGBARES INFORMATION-TERMINAL
DISPOSITIF A SEMI-CONDUCTEUR, PROCEDE DE REALISATION D'UN DISPOSITIF
ELECTRONIQUE, DISPOSITIF ELECTRONIQUE, ET TERMINAL D'INFORMATIONS
PORTABLE

PATENT (CC, No, Kind, Date): EP 1189282 A1 020320 (Basic)
WO 200171806 010927

...ABSTRACT A1

It is an object of the present invention to provide a low-cost semiconductor device including a **semiconductor chip** mounted on both surfaces of a wiring substrate without degrading electric characteristics, a method for manufacturing an electronic equipment, an **electronic equipment**, and a **portable** information terminal.

The semiconductor device includes projecting **electrodes** formed on one surface of a wiring substrate so as to have a prescribed height, a **semiconductor chip** having a thickness smaller than the height of the projecting **electrodes**, and an electronic component having a thickness larger than that of the **semiconductor chip** and mounted on the other surface of the wiring substrate so that the wiring substrate is warped to be recessed at the one surface. Thus, the rigidity as well as the spacing between the **semiconductor chip** and the mounting board are assured. Moreover, the semiconductor device having a logic LSI mounted on both surfaces of a wiring substrate is mounted on a mounting board in a housing with projecting **electrodes** having a prescribed height interposed therebetween, wherein the wiring substrate is warped to be recessed on the side having the projecting **electrodes**. Thus, the rigidity and the spacing are assured, whereby an **electronic equipment** and a **portable** information terminal are manufactured which cause no damage to the logic LSIs even when subjected to external pressure.

...CLAIMS A1

1. A semiconductor device, comprising: a wiring substrate including **electrodes** on a top surface and a **back** surface thereof; projecting **electrodes** formed on one surface of said wiring substrate so as to have a prescribed height; a **semiconductor chip** having a thickness smaller than said height of said projecting **electrodes** and mounted on said one surface of said wiring substrate so as to be electrically connected to said **electrodes** of said wiring substrate; and an electronic component having a thickness larger than that of said **semiconductor chip** and mounted on the other surface of said wiring substrate so as to be electrically connected to said **electrodes** of said wiring substrate so that said wiring substrate is warped to be recessed at said one surface.
2. The semiconductor device according to claim...

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...according to claim 1, wherein a value of a linear expansion coefficient of said electronic component is equal to or less than that of said **semiconductor chip**.

4. The **semiconductor** device according to claim 1, wherein the warping is bowl-shaped warping, and a difference in level between a central portion and a peripheral portion...

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34/TI,PN,PD,PY,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Chip Size Semiconductor Package and process for producing it
Chipgrosses Halbleitergehaue und seine Herstellung
Boitier semi-conducteur a largeur de puce et methode de fabrication
associee
PATENT (CC, No, Kind, Date): EP 997942 A2 000503 (Basic)
EP 997942 A3 010509

Chip Size Semiconductor Package and process for producing it
Boitier semi-conducteur a largeur de puce et methode de fabrication
associee

...ABSTRACT A2

A semiconductor device that meets the demand for realizing **semiconductor chips** in small sizes has connection lands (20) formed on an **electrode** terminal **carrying** surface of a **semiconductor chip** (10) which are electrically connected via a substrate (12) and solder bumps (26) to an external circuit. The connection lands (20) are electrically connected, through...

...to connection pads (22) formed on one surface of the interposing substrate (12) of an insulating material so as to face the connection lands (20). **Conductor** wiring patterns (24) inclusive of the connection pads (22) are formed on one surface of the interposing substrate (12). **Conductor** wiring patterns (30) inclusive of terminal lands on which the external connection terminals (26) will be mounted, are formed on the other surface of the interposing substrate (12). **Conductor** wiring patterns (24) formed on the one surface of the interposing substrate (12) are connected to the **conductor** wiring patterns (30) formed on the other surface of the interposing substrate (12) through solid vias (32) formed by filling recesses with a metal by plating. The recesses are formed to penetrate through the insulating material of the interposing substrate (12) by laser machining and this permits the **back** surfaces of the **conductor** wiring patterns (24) on the side of the insulating material to be exposed on their bottom surfaces so that these can be used as **electrodes** during the metal plating process.

CLAIMS 1. A semiconductor device comprising:

- a **semiconductor chip** having an **electrode** terminal **carrying** surface on which **electrode** terminals and **conductor** lands electrically connected to the **electrode** terminals are formed;
- an interposing substrate of an insulating material having a front surface and a back surface and disposed with the front surface facing the **electrode** terminal **carrying** surface of the **semiconductor chip**, in which a **conductor** wiring pattern, including **conductor** pads, is formed on the front surface, a **conductor** wiring pattern, including **conductor** lands, is formed on the back surface, external connection terminals

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are formed on the **conductor** lands on the **back** surface, and **conductor** vias composed of a plated metal filling viaholes extending through the interposing substrate electrically connect the **conductor** wiring pattern on the front surface and the **conductor** wiring pattern on the back surface; and bumps electrically connecting the **conductor** lands of the **semiconductor chip** to the **conductor** pads of the interposing substrate.

2. A semiconductor device according to claim 1, wherein the plated metal of the **conductor** vias consists of a low melting point alloy having a melting point of 300(degree)C or less.
3. A semiconductor device according to claim 1 or 2, wherein the **conductor** wiring pattern on the back surface is adhered to the back surface by a thermoplastic adhesive agent layer intervening therebetween.

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34/TI,PN,PD,PY,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Delay regulation circuit.

Schaltung zum Angleichen der Signalverzögerungszeiten.

Circuit de regulation des temps de propagation.

PATENT (CC, No, Kind, Date): EP 229726 A1 870722 (Basic)

EP 229726 B1 930616

...CLAIMS B1

1. Apparatus formed on a **semiconductor chip** fabricated to **carry** a plurality of **electronic** circuits, each of **which includes** a respective output stage having an output terminal for providing an output current thereat in response to an input signal applied to that output stage...
- ...response time delay between an input signal applied to the base of the emitter follower transistor (Q24) and an output signal thereat to increase current **conduction** of the second transistor (Q29).
3. Apparatus as claimed **in claim 2** wherein the emitter follower transistor (Q24) includes a base lead for receiving said input signal and said control means includes a third transistor (Q28) having a **base lead** connected to the base lead of the emitter follower transistor (Q24), and an emitter lead connected to a voltage potential (6Rd) via the series circuit of a diode (D1) and a resistor (R6) to develop a control signal which is connected to the second transistor (Q29) for **controlling** current **conduction** thereof.

09/26/2002 09/939,457

37/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Chip size package **semiconductor** device and method of
manufacturing the same
Halbleitervorrichtung in Chip-Grosse und Verfahren zu deren Herstellung
Dispositif semi-**conducteur** ayant la taille d'une puce et son procede
de fabrication

PATENT (CC, No, Kind, Date): EP 1152464 A2 .011107 (Basic)

.ABSTRACT A2

In order to have a thin type **semiconductor chips** featuring
a high yield and a low cost in production, an excellent packaging
reliability, and a robust structure against damages, there is provided a
method...

...to a processing, then loses it after the processing; bonding
non-defective LSI chips on the adhesive sheet, with their device surfaces
facing downward; uniformly **coating an insulating film**
on the non-defective LSI chips; uniformly grinding the **insulating**
film to a level of the bottom surfaces of these LSI chips; applying
a predetermined process to the adhesive sheet to weaken its adhesive
strength thereof...

...CLAIMS A2

1. A chip-like electronic component having at least its all
electrodes formed on one surface thereof, a side wall thereof
being covered with a protective material, and another surface
opposite to said one surface fabricated to...

...comprises either one of an organic insulating resin and an inorganic
insulating material.

3. The chip-like electronic component according to claim 1, comprising a
semiconductor chip diced at a position of said protective
material for mounting on a packaging substrate, wherein said
electrode is formed on a device surface, and a whole area of
said side wall thereof is covered with said protective material.

4. The chip-like electronic component according to claim 3, wherein a
solder bump is formed on said **electrode**.

5. The chip-like electronic component according to claim 1, wherein a
plurality of a same or different types of **semiconductor**
chips are bonded and integrated by said protective material.

6. A pseudo wafer comprising a plurality of a same or different types of
chip-like electronic components each having at least all their
electrodes formed on one surface thereof, bonded with each
other with a protective material coated therebetween, and another
surface opposing said one surface being fabricated to...

...adhesive strength prior to a processing and to lose said adhesive
strength after said processing;
fixing a plurality of a same or different types of **semiconductor**
chips on said adhesive material with an **electrode** surface
thereof facing down;

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coating a whole area including said plurality of the same or different types of **semiconductor chips** and a gap therebetween with a protective material;
removing said protective material from a side thereof opposite to said **electrode** surface to a level of a bottom surface of the **semiconductor chips**;
applying a predetermined process to said adhesive material to weaken said adhesive strength of said adhesive material so as to peel off a pseudo wafer on which said plurality of the same or different types of **semiconductor chips** are bonded; and
dicing said plurality of the same or said different types of **semiconductor chips** into each **semiconductor chip** or each **chip**-like electronic component by cutting said protective material in said gap therebetween.

11. The method of manufacturing a chip-like electronic components according to claim 10, wherein:
said substrate has a flat surface;
said adhesive material is an adhesive sheet;
said plurality of the same or different types of **semiconductor chip** bonded on said adhesive sheet are non-defective;
said protective material is either one of an organic insulating material and an inorganic insulating material, and is uniformly coated on said **semiconductor chips** from bottom surfaces thereof to be hardened;

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37/TI,PN,PD,PY,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Method of forming an electrical connection for an integrated circuit
Verfahren zur Herstellung einer elektrischen Verbindung für eine
integrierte Schaltung
Procede de fabrication d'une connection electrique pour une puce de circuit
integre

PATENT (CC, No, Kind, Date): EP 482940 A1 920429 (Basic)
EP 482940 B1 960327

...ABSTRACT A1

A film carrier type semiconductor device according to the present invention comprising a carrier type (6) and a **semiconductor chip** (2) attached thereto has the feature that connection of each **electrode** terminal on the semi-conductor chip and the corresponding lead (4) on the carrier tape is made, instead of by pressing a **bump** on the **electrode** terminal and the corresponding lead together, or the like, through the intervention by the hollow cylindrical **conductor layer** lining the corresponding through hole (13) formed in the carrier tape (6) and solder (4) filling it. After alignment between the lead and the through hole, the solder is caused to melt once and solidified with the result of completing the connection between the **electrode** terminal and the lead.

The advantage of invention resides in that the formation of bumps as of Au and bonding under heat and pressure accompanied by thermal stress, or the like, are needless, and the **semiconductor chip** is not subjected to heating except the period of keeping the solder molten, accordingly enabling improvement in reliability and **reduction** in fabrication **cost** of the film carrier type semiconductor device.
(see image in original document)

...CLAIMS A1

1. A film carrier type semiconductor device comprises a carrier tape of film (6) made of an insulating material and **carrying** thereon a number of leads (4) formed on said carrier tape, and a **semiconductor chip** (2) attached to said carrier tape, said leads consisting of inner leads extending into and outer leads extending away from the corresponding area of said carrier tape to said **semiconductor chip**, said carrier tape being provided with through holes (13) each at the ends of said inner leads, respectively, each through hole being lined with a hollow cylindrical **conductor layer** connected with the end of the corresponding lead and filled with solder (14), and said hollow cylindrical **conductor layer** being electrically connected to the corresponding one of **electrode** terminals on said **semiconductor chip** through intervention by said solder filling said hollow **conductor** cylindrical **layer** by the reflow process.
2. A film carrier type semiconductor device according to claim 1, wherein said through holes are correspondent in location to the **electrode** terminals of said semi-conductor chip.

3. A **film** carrier type semiconductor device according to claim 1 or claim 2, wherein a solder layer is formed on each **electrode** terminal of said **semiconductor chip** before said reflow process. ...

...CLAIMS B1

1. A method of fabricating a film carrier tape semiconductor device comprising the steps of:
providing an **insulating film** carrier tape (6), with a plurality of leads (4) formed on said insulating tape, each of said leads consisting of an inner lead portion and an outer lead portion, a plurality of through holes (13) each provided in an end of a said inner lead, and a tubular **conductor layer** on the wall of each through hole in contact with said inner lead portion;
assembling said carrier tape with a **semiconductor chip** (2) having thereon a plurality of **electrode** terminals (15) such that each of the **electrode** terminals of said **semiconductor chip** is aligned with an associated one of said through holes of said carrier tape; and characterised by providing solder (14) in the form of a paste in each of said through holes before assembling the carrier tape with the **semiconductor chip**; and
reflowing the solder in said through holes thereby to connect each of said **electrode** terminals (15) of said **semiconductor chip** to the **conductor layer** in the associated through hole.
2. The method as claimed in Claim 1, wherein each of said **electrode** terminals of said **semiconductor chip** is coated with a barrier layer.
3. The method as claimed in Claim 2, wherein a solder bump is formed on said barrier layer.
- 4...

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37/TI,PN,PD,PY,K/3 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

RECONFIGURABLE MULTICHIP MODULE STACK INTERFACE
INTERFACE D'EMPILEMENT POUR MODULE MULTIPUCE RECONFIGURABLE
Patent and Priority Information (Country, Number, Date):

Patent: WO 200108187 A1 20010201 (WO 0108187)
Publication Year: 2001

.chips may be located with electrical connections provided between chips as well as to external components. Most commonly, these multichip modules are incorporated in multi-layer dielectric substrates that employ thin film processes for forming electrically conductive traces to interconnect the various chips. The multi-layer dielectric substrates are made employing techniques that have been initially developed for various types of semiconductive type processing. These MCMS may include high density interconnect (HDI)...a plurality of electronic components wherein each of these components has at least one external electrical contact. Running through each of the electronic components are conductive traces which comprise a feedback circuit over which predetermined current may be transmitted such that a voltage drop over the circuit may be measured. This...elements which may be used in computer systems for aircraft and spacecraft. Electronic assembly 10 may include a number of electronic processing components as well as conductive pathways for routing signals to and from the components, as well as to remotely locate computer systems. The electronics assembly disclosed in Fig. 1 includes a multichip module (MCM) 14 which is configured to hold a number of electronic processing components, such as semiconductor chips. Further included in the module are conductive traces for establishing electrical communications between the chips, as well as between the IP chips and external systems. MCM's perform the functions of...

39/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Chip-like electronic components, a method of manufacturing the same, a
pseudo wafer therefor and a method of manufacturing thereof
Elektronische Bauteile in Chipform und Verfahren zu ihrer Herstellung, eine
Pseudo Wafer dafur und Verfahren zu dessen Herstellung
Composant electronique en forme de pastille, son procede de fabrication,
une pseudo plaquette et son procede de fabrication
PATENT (CC, No, Kind, Date): EP 1150552 A2 011031 (Basic)

...ABSTRACT A2

A method of manufacturing the **semiconductor chips** comprises
the steps of: pasting on a substrate an adhesive sheet having a property
to retain its adhesive strength prior to a processing, then lose its
adhesive strength after the processing; fixing a plurality of
non-defective bare chips on this adhesive sheet, with their Al
electrode pad surfaces facing down; **coating a resin** on
a whole area other than the Al **electrode** pad surfaces of the
plurality of non-defective bare chips including interspaces therebetween;
applying a predetermined process to the adhesive sheet to weaken its
adhesive...

...CLAIMS A2

1. A chip-like electronic component having at least its **electrodes**
formed exclusively on one surface thereof, and surfaces other than
said one surface are continuously covered with a protective material.

2. The chip-like electronic...

...said protective material comprises an organic insulating resin or an
inorganic insulating material.

3. The chip-like electronic component according to claim 1, comprising a
semiconductor chip diced from a wafer at a position of
said protective material for mounting on a package substrate, wherein
said **electrode** is formed on said one surface, which is a device
surface, of said **semiconductor chip**, and both a side wall
and a bottom surface of said **semiconductor chip** are
covered with said protective material.

4. The chip-like electronic component according to claim 3 wherein a
solder bump is formed on said **electrode**.

5. The chip-like electronic component according to claim 1 wherein a
plurality and/or a plurality of different types of
semiconductor chips are integrated as bonded by said
protective material.

6. A pseudo wafer comprising a plurality and/or a plurality of different
types of chip-like electronic components having at least their
electrodes formed solely on one surface thereof, wherein
interspaces between said plurality and/or said plurality of different
types of chip-like electronic components and bottom...

...resin and an inorganic insulating material.

8. The pseudo wafer according to claim 6 wherein said plurality and/or

said plurality of different types of **semiconductor chips** arrayed thereon are diced at a position of said protective material between said plurality of **semiconductor chips** and fabricated into a discrete **chip** or an integrated **semiconductor chip** integrating a plurality and/or a plurality of different types of **semiconductor chips** to be mounted on a packaging substrate.

9. The pseudo wafer according to claim 8 wherein a solder bump is formed on said **electrode**.

10. A method of manufacturing a chip-like electronic component, comprising the steps of:
pasting an adhesive material on a substrate, said adhesive material having...

...strength prior to a processing and to lose said adhesive strength after said processing;

fixing a plurality and/or a plurality of different types of **semiconductor chips** on said adhesive material with an **electrode** surface thereof facing down;

coating a whole area including said plurality and/or said plurality of different types of **semiconductor chips** and interspaces therebetween with a protective material;

applying a predetermined process to said adhesive material to weaken said adhesive strength of said adhesive material so as to peel off a pseudo wafer which bonds said plurality and/or said plurality of different types of **semiconductor chips** as covered with said protective material; and

dicing said plurality and/or said plurality of different types of **semiconductor chips** by cutting said protective material in said interspaces therebetween thereby obtaining a discrete **semiconductor chip** or a **chip**-like electronic component.

09/26/2002 09/939,457

39/TI,PN,PD,PY,K/2 (Item 2 from file: 348)
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Semiconductor plastic package and process for the production thereof
Kunststoffhalbleitergehaeuse und seine Herstellung
Boitier plastique pour semi-**conducteur** et procede de fabrication
associe

PATENT (CC, No, Kind, Date): EP 926729 A2 990630 (Basic)
EP 926729 A3 991208

...ABSTRACT A2

A semiconductor plastic package excellent in heat diffusibility and free of moisture absorption, structured by fixing a **semiconductor chip** on one surface of a printed circuit board, connecting a semiconductor circuit **conductor** to a signal propagation circuit **conductor** formed on a printed circuit board surface in the vicinity thereof by wire bonding, at least connecting the signal propagation circuit **conductor** on the printed circuit board surface to a signal propagation circuit **conductor** formed on the other surface of the printed circuit board or a connecting **conductor** pad of a solder ball with a through-hole **conductor**, and encapsulating the **semiconductor chip** with a resin, the printed circuit board having a metal sheet of nearly the same size as the printed circuit board nearly in the center in the thickness direction of the printed circuit board, the metal sheet being insulated from **front** and reverse circuit **conductors** with a heat-resistant resin composition, the metal plate being provided with a clearance hole having a diameter greater than the diameter of each of...

...the metal sheet, one surface of the metal sheet being provided with at least one protrusion portion which is of the same size as the **semiconductor chip** and exposed on a surface, the **semiconductor chip** being fixed on the protrusion portion.

CLAIMS 1. A semiconductor plastic package structured by fixing a **semiconductor chip** on one surface of a printed circuit board, connecting a semiconductor circuit **conductor** to a signal propagation circuit **conductor** formed on a printed circuit board surface in the vicinity thereof by wire bonding, at least connecting the signal propagation circuit **conductor** on the printed circuit board surface to a signal propagation circuit **conductor** formed on the other surface of the printed circuit board or a connecting **conductor** pad of a solder ball with a through-hole **conductor**, and encapsulating the **semiconductor chip** with a resin,

...to any one of the preceding claims, wherein the heat-resistant resin composition is a thermosetting resin composition containing a polyfunctional cyanate ester or a **prepolymer** of said cyanate ester as an essential component.

6. A semiconductor plastic package structured by fixing a **semiconductor chip** on one surface of a printed circuit

board, connecting a semiconductor circuit **conductor** to a signal propagation circuit **conductor** formed on a printed circuit board surface in the vicinity thereof by wire bonding, at least connecting the signal propagation circuit **conductor** on the printed circuit board surface to a signal propagation circuit **conductor** formed on the other surface of the printed circuit board or a connecting **conductor** pad of a solder ball with a through-hole **conductor**, and encapsulating the **semiconductor chip** with a resin,

the printed circuit board having a metal sheet of nearly the same size as the printed circuit board nearly in the center in the thickness direction of the printed circuit board, the metal sheet being insulated from **front** and reverse circuit **conductors** with a heat-resistant resin composition, the metal plate being provided with a clearance hole having a diameter greater than the diameter of each of...

...the metal sheet, one surface of the metal sheet being provided with at least one protrusion portion which is of the same size as the **semiconductor chip** and exposed on a surface, the **semiconductor chip** being fixed on the protrusion portion, the other surface of the metal sheet being provided with a protrusion surface exposed for diffusing heat.

...center in the thickness direction of the printed circuit board, providing at least one exposed metal sheet protrusion of nearly the same size as a **semiconductor chip** on one surface of the printed circuit board, fixing the **semiconductor chip** thereon, connecting the **semiconductor chip** to a signal propagation circuit **conductor** formed on a printed circuit board surface in the vicinity thereof by wire bonding, at least connecting the signal propagation circuit **conductor** on the printed circuit board surface to a signal propagation circuit **conductor** formed on the other surface of the printed circuit board or a connecting **conductor** pad of a solder ball with a through-hole **conductor**, and encapsulating the **semiconductor chip** with a resin,

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39/TI,PN,PD,PY,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Method of connecting TAB tape to **semiconductor chip**
Verfahren zum Verbinden eines TAB-Bandes an einem Halbleiterchip
Procede pour la connexion d'une bande TAB a une puce semi-conductrice
PATENT (CC, No, Kind, Date): EP 427384 A2 910515 (Basic)
EP 427384 A3 920102
EP 427384 B1 990428

Method of connecting TAB tape to **semiconductor chip**
Procede pour la connexion d'une bande TAB a une puce semi-conductrice

...ABSTRACT A2

A method of connecting a TAB tape (12) to a **semiconductor chip** (1) is disclosed which comprises the steps of preliminarily locating and fixing bumps (6) at positions corresponding to a pattern of **electrodes** (7) of the **semiconductor chip** to be connected; and bonding the bumps by thermocompression to the **electrodes** of the **semiconductor chip** and the leads (2) of the TAB tape, respectively, so that each **electrode** of the **semiconductor chip** is electrically connected to the corresponding lead of the TAB tape through a corresponding one of the bumps. Also disclosed are a bump sheet (11) and a bumped tape to be used in a method of connecting a TAB tape to a **semiconductor chip**.

CLAIMS 1. A method of connecting a TAB tape (12) to a **semiconductor chip** (1) comprising the steps of:

- (a) preparing spherical bumps (6);
- (b) preliminary locating said bumps (6) on a substrate (11; 22; 31) at positions corresponding to a pattern of **electrodes** (7) of the **semiconductor chip** to be connected, wherein said substrate (22, 31) is provided with through-holes (24) at said positions, and wherein the diameter of the through-holes...

...6)

- (c) fixing said bumps (6) to portions of leads (2) of the TAB tape; and
- (d) bonding said bumps (6) by thermocompression to the **electrodes** (7) of the **semiconductor chip**, respectively, so that each **electrode** of the **semiconductor chip** is electrically connected to the corresponding lead (2) of the TAB tape through a corresponding one of the bumps.

2. A method according to claim...

...of claims 1 to 3, wherein the substrate (22) is made of metal and is provided with an upper substrate (40) made of a synthetic **resin film** (40) both provided with through-holes at said positions.

5. A method according to claim 4, wherein the bumps (6) are fixed on the upper...

...a bump sheet and the leads (2) of said TAB tape (12) are formed in a predetermined pattern directly on one surface of said synthetic

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resin film of said bump sheet in an electrically **conducting** relation with said **bumps**.

6. A method according to claim 4 or 5, wherein
 - (a) the bumps (6) are mechanically pushed into the through-holes of the **resin film** forming the upper substrate (40), and
 - (b) peeling-off the synthetic **resin film carrying** the bumps (6).
7. A method according to claim 4 or 5, comprising the steps of:
 - (a) adding a solution of synthetic resin (40) to the substrate (22) **carrying** the preliminarily located bumps (6), and
 - (b) solidifying the synthetic resin and peeling-off the solidified synthetic **resin film carrying** the bumps (6).
8. A method according to any one of claims 4 to 7, wherein the portions of leads (2) of the TAB tape are formed directly on one surface of the synthetic **resin film carrying** the bumps (6) by means of copper-plating.
9. A method of connecting a TAB tape (12) to a **semiconductor chip** (1) comprising the steps of:
 - (a) preparing spherical bumps (6);
 - (b) preliminary locating said bumps (6) on a substrate (11; 22; 31) at positions corresponding to a pattern of **electrodes** (7) of the **semiconductor chip** to be connected, wherein said substrate (22, 31) is provided with through-holes (24) at said positions;

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41/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Flip **chip** assembly structure for **semiconductor** device and
method of assembling therefor
Flip-Chip Aufbau-Struktur fur Halbleitervorrichtung und deren
Aufbauverfahren
Structure d'assemblage tete-beche (dite "flip-**chip**") pour dispositif
semiconducteur et son procede d'assemblage
PATENT (CC, No, Kind, Date): EP 1205970 A2 020515 (Basic)

...ABSTRACT A2

A semiconductor device includes a **semiconductor chip** (1)
and a printed circuit board (4). Metal **electrodes** (2) of the
semiconductor chip (1) and the internal connection terminals
(5) of the printed circuit board (4) are electrically connected through
the metallic joining via precious metal bumps (3...

...CLAIMS A2

1. Flip chip assembly structure comprising:
a **semiconductor chip** (1) having a circuit for processing
electrical signals;
electrodes provided (2) on said **semiconductor chip**;
bumps (3) which are respectively formed on said **electrodes** (2);
internal connection terminals (5) through which the electrical signal is
fetched via the associated ones of said bumps from the associated
ones of said **electrodes**
5. Flip chip assembly structure comprising:
a **semiconductor chip** (1) having a circuit for processing
electrical signals;
electrodes (2) provided on said **semiconductor chip**;
precious metal bumps (3) which are respectively formed on said
electrodes;
14. A method of loading a **semiconductor chip** (1) on a printed
circuit board (4) in a face down manner, a flip chip assembly method
comprising: the process of forming precious metal bumps (3) on
electrodes (2) of said **semiconductor chip** (1); the
process of placing a semi-cured resin sheet containing 50 vol% or
more inorganic fillers on a predetermined position on said printed
circuit board to load thereon said **semiconductor chip**
with said precious metal bumps aligned with internal connection
terminals of said printed circuit board; and the process of after
having applied from the rear face side of said **semiconductor**
chip (1), the heat, the load and the ultrasonic wave by a
joining tool to push said precious metal bumps into said resin sheet
and processing said precious metal bumps thereagainst to join
compressively said precious metal bumps to a precious metal film
formed on said internal connection terminals, **carrying** out the
heating processing to cure said resin sheet.

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41/TI,PN,PD,PY,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Connection structure for connecting a display module and a printed substrate by using a semiconductor device
Verbindungsstruktur zwischen einem Anzeigemodul und einem bedruckten Substrat unter Verwendung einer Halbleitervorrichtung
Structure de connexion d'un module d'affichage et d'un substrat imprime en utilisant un dispositif semiconducteur
PATENT (CC, No, Kind, Date): EP 1185057 A2 020306 (Basic)

...CLAIMS substrate (15, 17, 18), said display module (1, 20, 25) including a display panel (2) connected with a semiconductor device (3, 21, 26) having a **semiconductor chip** (4) mounted on a flexible wiring substrate (3a), wherein:
said display module (1, 20, 25) is fixed to a housing member (7) in a folded state with respective rear surfaces of said semiconductor device (3, 21, 26) and said display panel (2) facing each other;
a **protruding electrode** (6, 22, 27) is formed on said semiconductor device (3, 21, 26);
said display module (1, 20, 25) is fixed to said printed substrate (15
...

...holding member (11) attached to said housing member (7), said holding member (11) supporting said printed substrate (15, 17, 18) in engagement therewith; and
said **protruding electrode** (6, 22, 27) formed on said semiconductor device (3, 21, 26) is in contact with a connection terminal (16, 23, 29) provided on said printed substrate (15, 17, 18) corresponding to said **protruding electrode** (6, 22, 27).
2. The connection structure for a display module (1, 20, 25) and a printed substrate (15, 17, 18) of claim 1,
5, 17, 18) having a connection terminal (16, 23, 29), comprising:
a semiconductor device (3, 21, 26) which includes a flexible wiring substrate (3a), a **semiconductor chip** (4) mounted on said flexible wiring substrate (3a), and a **protruding electrode** (6, 22, 27) which establishes electrical connection with said connection terminal (16, 23, 29) of said printed substrate (15, 17, 18); and
a display panel...

...includes a semiconductor device (3, 21, 26) and a display panel (2),
said semiconductor device (3, 21, 26) including a flexible wiring substrate (3a), a **semiconductor chip** (4) mounted on the flexible wiring substrate (3a), and a **protruding electrode** (6, 22, 27) which establishes electrical connection with said connection terminal (16, 23, 29) of said printed substrate (15, 17, 18); said display panel (2...

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41/TI,PN,PD,PY,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor device and manufacturing method thereof
Halbleiter und seine Herstellung
Dispositif a semi-**conducteur** et methode de fabrication associee
PATENT (CC, No, Kind, Date): EP 1045443 A2 001018 (Basic)

Dispositif a semi-**conducteur** et methode de fabrication associee

...ABSTRACT A2

When a first **semiconductor chip** is installed on a circuit substrate by using an anisotropic **conductive** bonding agent, one portion thereof is allowed to protrude outside the first **semiconductor chip**. A second **semiconductor chip** is installed on the first **semiconductor chip** and a support portion formed by the protruding resin. The protruding portion of the second **semiconductor chip** is supported by the support portion from under. Thus, in a semiconductor device having a plurality of laminated **semiconductor chips** in an attempt to achieve a high density, even when, from a **semiconductor chip** stacked on a circuit substrate, one portion of a **semiconductor chip** stacked thereon protrudes, it is possible to **carry** out a better wire bonding process on **electrodes** formed on the **protruding** portion.

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41/TI,PN,PD,PY,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor package for flip-**chip** mounting process
Halbleiterpackung fur Flipchipmontage
Empaquetage semi-**conducteur** pour le procede de montage a pastille
renversee
PATENT (CC, No, Kind, Date): EP 732736 A2 960918 (Basic)
EP 732736 A3 961030

Semiconductor package for flip-**chip** mounting process
Empaquetage semi-**conducteur** pour le procede de montage a pastille
renversee

...ABSTRACT A3

A semiconductor device comprising a base member (26) **carrying** thereon a **semiconductor chip** (20) via an interconnection pattern (27a) provided on an upper major surface of the base member, the **semiconductor chip** (20) **carrying** solder bumps (22) on a lower major surface thereof facing the upper major surface of the base member (26), such that the solder bumps establish a contact with the interconnection pattern (27a). The **semiconductor chip** (20) further carries an **electrode** pad (23) on the lower major surface, the **electrode** pad (23) having a melting temperature exceeding a melting temperature of the solder bumps and having a thickness (h) smaller than a height (H) of...

3. A semiconductor device as claimed in claim 1 or 2, wherein said semiconductor device further includes a cap (30) covering said **semiconductor chip** (20), said cap (30) being mounted upon said upper major surface of said base member (26) by a bonding layer (29) and hermetically sealing said **semiconductor chip** (20) therein, said cap (30) thereby **carrying** said **semiconductor chip** (20) on an inner surface thereof.
4. A semiconductor device as claimed in anyone of claims 1 - 3, wherein said semiconductor device further includes an interconnection substrate (27) on said upper major surface of said base member (26), said interconnection substrate (27) **carrying** said interconnection pattern (27a). ...

09/26/2002 09/939,457

41/TI,PN,PD,PY,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor package stack module and method of producing the same
Stapelmodul von Halbleiterpackungen und Herstellungsverfahren
Module a empilement d'empaquetages de semi-conducteurs et procede de
fabrication

PATENT (CC, No, Kind, Date): EP 729184 A2 960828 (Basic)
EP 729184 A3 991103

13. A semiconductor package as claimed in claim 12, further comprising an insulator covering terminal **electrodes** formed on a **front** of an uppermost layer of said semiconductor package.
14. A semiconductor package as claimed in claim 1, further comprising a **conductor layer** formed on and along edge portions of said carrier and connected to ground.
15. A semiconductor package as claimed in claim 1, further comprising through...

- ...said ceramic carrier substrate by one of polishing, grinding, surface grinding, and etching; and
(d) stacking and soldering a plurality of ceramic carrier substrates each **carrying** a respective LSI **chip**.
31. In a **semiconductor** package stack module, a multicarrier body formed with a plurality of carriers not separated from each other is subjected to mounting of LSI chips, connection...

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41/TI,PN,PD,PY,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Micromechanical atomic force sensor head.
Mikromechanische Fuhlervorrichtung fur atomare Krafte.
Dispositif micromecanique detecteur de forces atomiques.
PATENT (CC, No, Kind, Date): EP 262253 A1 880406 (Basic)

...ABSTRACT gap between said bulges (45, 46) being adjustable by means of electrostatic forces generated by a potential (V (sub(d))) applied to a pair of **electrodes** (41, 43) respectively **coated** onto parallel surfaces of said beams (40, 44).

The sensor head consists of one single piece of semiconductor material, such as silicon or gallium arsenide (or any other compounds thereof) which is fabricated to the dimensions required for the application by means of conventional **semiconductor chip** manufacturing techniques.

49/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

PRINTED WIRING BOARD, METHOD OF PRODUCING THE SAME AND ELECTRONIC DEVICES
LEITERPLATTE, VERFAHREN ZU DEREN HERSTELLUNG UND ELEKTRONISCHE
VORRICHTUNGEN
CARTE A CIRCUIT IMPRIME, SON PROCEDE DE PRODUCTION ET DISPOSITIFS
ELECTRONIQUES

PATENT (CC, No, Kind, Date): EP 779772 A1 970618 (Basic)
EP 779772 A1 980729
WO 9610326 960404

...ABSTRACT together into a unitary body by means of a bonding agent or thermal fusing. Formed on the surface of the insulating board (11) is a **conductor** pattern (17) that continuously runs across the fold at the cutout portion between the first portion and the second portion, and thus the **conductor** pattern assuring continuity between both sides of a printed wiring board (20) results without the need for providing through-holes. By employing such a printed wiring board, a compact and low-cost feature is implemented into **electronic apparatuses** or **portable information apparatuses** such as liquid crystal display devices or electronic printers, through a miniature, light-weight and flat design effort.

5. The printed wiring board according to claims 3 or 4, wherein said cutout portion is made up of a plurality of...

...material or a mixture of materials or a combination of materials selected from epoxy-based resin, polyimide-based resin, BT based resin and polyester-based **resin**.

10. A multi-layered printed wiring board comprising a pair of outer **layers** made of **insulating** material, one or more inner **layers** made of **insulating** material sandwiched between the outer **layers**, and **conductor** patterns formed between the neighboring outer layers and inner layers, one of the outer layer having a first portion that is attached onto the neighboring...

...said one of the outer layer having a cutout portion that is formed by cutting out partly the insulating material along the fold, wherein a **conductor** pattern is formed on top of said one of the outer **layer**, said **conductor** pattern continuously extending across the fold at the cutout portion between the first portion and the second portion.

11. A manufacturing method of a printed...

...the insulating board material along the fold that partitions the insulating board into a first portion and a second portion, forming and then patterning a **conductive film** on the surface of the insulating board to form a **conductor** pattern that continuously extends across the fold at the cutout portion between the first portion and the second portion, and folding the insulating board along the fold with its **conductor** pattern side out, whereby the first portion and the second portion are mutually

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49/TI,PN,PD,PY,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

A hybrid IC.

Integrierte Hybridschaltung.

Circuit integre hybride.

PATENT (CC, No, Kind, Date): EP 683519 A2 951122 (Basic)
EP 683519 A3 980513

...ABSTRACT A2

On a ceramic substrate, spiral-type inductors of a single layer wiring of a metal thin film are provided and respectively **connected** to a wiring pattern formed on another face of the substrate via through holes. A **semiconductor chip** is flip-chip mounted on the substrate in a face-down manner. On the face of the **semiconductor chip**, capacitors composed of a highly dielectric material, resistors formed by an ion implantation method or a thin-film forming method, and FETs are provided, respectively. **Interconnection** between the substrate and an external **circuit board** is achieved employing terminals formed at end faces of the substrate. The terminals have a concave shape with respect to the end face of the substrate. Thus, there is no need to use a package, and miniaturization and **reduction** in **cost** of a high-performance hybrid IC is achieved. (see image in original document)

...CLAIMS A2

1. A hybrid IC comprising:
 - a substrate;
 - at least one inductor formed on the substrate;
 - a **semiconductor chip** mounted on the substrate by flip-chip bonding;
 - at least one terminal formed in a predetermined portion of an outer periphery of the substrate,
 - wherein the **semiconductor chip** comprises a plurality of circuit elements provided therein, at least one of the plurality of circuit elements being an MIM capacitor having a metal-**insulation film-metal** (MIM) structure, the **insulation film** being composed of a highly dielectric material.
2. A hybrid IC according to claim 1 further comprising at least one matching circuit for matching an input signal to the circuit elements provided inside the **semiconductor chip**, the matching circuit comprising at least one inductor.
3. A hybrid IC according to claim 2, wherein a wiring pattern is formed of a single metal layer on both faces of the substrate, the wiring patterns on the respective faces of the substrate being **interconnected** with each other via through holes, and the at least one inductor comprised in the matching circuit is formed in the wiring pattern on one...

...inductor.

7. A hybrid IC according to claim 2, wherein the matching circuit comprises an inductor and a capacitor, the capacitor being formed

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A direct chip attach module (DCAM).
Modul zur direkten Befestigung von Chips (DCAM).
Module d'attachement direct de puces (DCAM).
PATENT (CC, No, Kind, Date): EP 592022 A1 940413 (Basic)

...ABSTRACT A1

A low cost Surface Mount Carrier (SMC) for **carrying** integrated circuit chips mounted thereon. The carrier, or interposer, is a thin-small single layer or, a multi-layer deck of **printed circuit board** (FR-4) material with at least one direct chip attach (DCA) site for mounting a **semiconductor chip**. The DCA site has chip bonding pads wherein the integrated circuit chip's pads are wire bonded to or soldered to the carrier. The bonding pads are **connected** to wiring pads through interlevel vias and wiring lands or traces which may be on one of several wiring planes. The carrier is **connected** to the next level of packaging through the wiring pads.
(see image in original document)

.power and said signals to said at least one integrated circuit chip,
said distribution means comprised of a plurality of lands, and, at least one **layer** of a **resin** fiberglass composite material.

2. The carrier of claim 1 wherein the distribution means further comprises:
a plurality of **conductive** planes, said plurality of lands being located on said **conductive** planes;
each adjacent pair of said **conductive** planes being separated by one of said at least one layer; and, a plurality of interlevel vias.
3. The carrier of claim 2 wherein at least one of said plurality of **conductive** planes is an internal **conductive** plane.
4. The carrier of claim 3 wherein said internal **conductive** plane is a power distribution plane and/or a signal distribution plane.
5. The carrier of any of claims 1-4 wherein said at least one layer includes a plurality of **insulating layers**, each said **insulating layer** being sandwiched between a pair of said plurality of **conductive** planes.
6. The carrier of any of claims 1-5 wherein the distribution means further comprises a plurality of chip bonding pads and a plurality of carrier pads.
12. The integrated circuit chip module of claim 11 wherein said at least one **conductive** plane comprises a plurality of **conductive** planes, and, each adjacent pair of said **conductive** planes being separated by one said at least one layer.
13. The integrated circuit chip module of claim 11 or 12 wherein at least two of said plurality of **conductive** planes are internal **conductive** planes and said at least one layer is a plurality of **insulating layers**, whereby each said **insulating layer** is sandwiched between a pair of said **conductive**

planes.

14. The integrated circuit chip module of any of claims 11-13 wherein the chip mounting means comprises a deposited solder ball on each said chip bonding pad, whereby said deposited solder balls fixedly attach and electrically **connect** said each chip to said carrier.
15. The integrated circuit chip module of any of claims 11-14 wherein each said integrated circuit chip has...

...is fixedly mounted in said cavity.

17. An integrated circuit package comprising:
 - a carrier, said carrier comprising:
 - a plurality of wiring planes,
 - a plurality of **insulating layers** of **resin** fiberglass composite material, each said **insulating layer** being sandwiched between an adjacent pair of said wiring planes,
 - a plurality of vias, each of said vias extending from a one of said wiring planes through at least one of said **insulating layers** to a second of said wiring planes,
 - a plurality of carrier pads, and
 - at least one chip mounting location on a surface of said carrier...

49/TI,PN,PD,PY,K/4 (Item 4 from file: 348)
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Semiconductor chip carrier and method of making it.
Halbleiterchiptrager und Verfahren zu dessen Herstellung.
Support pour puce semi-**conductrice** et procede pour sa fabrication.
PATENT (CC, No, Kind, Date): EP 359513 A2 900321 (Basic)
EP 359513 A3 901219

...ABSTRACT A2

A **semiconductor chip** carrier for **carrying** a single chip (15) and having a built-in capacitor, comprises a ceramic insulator body (2) having first and second opposite main faces, and a plurality of **conductor** lines (6,7) comprising power lines, ground lines and signal lines for forming **connections** to said chip extending through said ceramic body (2) from one main face to the other. A **layer** (3) of ceramic **dielectric** material is embedded in said ceramic body remote from said main faces, and **electrode layers** embedded in the ceramic body (2) contact the capacitor layer (3), to form the built-in capacitor. The power and ground lines (16) pass through and contact the capacitor layer (3) and are **connected** to said **electrodes** so that said capacitor provides capacitance between the power lines and the ground lines. To minimize noise generation and improve signal processing speed, the signal...

...CLAIMS A3

1. A ceramic **semiconductor chip** carrier for **carrying** a single chip (15) and having a built-in capacitor (3;43) providing capacitance between **conductor** lines comprising power, ground and signal lines (6,7;47,48) for the chip extending through the carrier, said capacitor being formed by at least one **dielectric layer** (4;44) and **electrodes** (5;46) embedded in the carrier, said power and ground lines (4;47) passing through said **dielectric layer** (4;44) making contact therewith and being **connected** to said **electrodes** (5;46) at the faces of the **dielectric layer** so that the capacitance is between the power lines and the ground lines, characterized in that said signal lines (7;48) extend past the **dielectric layer** (4;44) without contacting it at locations spaced laterally from it.
2. A **semiconductor chip** carrier according to claim 1 having a ceramic insulator body (2;42) in which said capacitor layer (4;44) of ceramic dielectric material is embedded remote from opposed main faces of said body (2), the **electrodes** (5) being **electrode layers** embedded in said ceramic body (2) and contacting said capacitor layer (4).

.larger area than said at least one green sheet (10;44) of dielectric material, such that on assembly and firing of said green sheets some **conductor** lines formed do not pass through said capacitor **layer** and other **conductor** lines formed do pass through said capacitor layer, said green sheets further **carrying electrode-forming material** (14;46) for forming **electrodes** adjacent said capacitor **layer** and contacting said

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conductor lines which do pass through said capacitor layer.

27. A combination of green sheets according to claim 26 wherein there are more than two said green sheets (8;42) of insulator material and two of said sheets of insulator material **carry** said **electrode**-forming material.

28. A combination of green sheets according to claim 26 further comprising at least two intermediate sheets (45) of composition different from that...

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49/TI,PN,PD,PY,K/5 (Item 5 from file: 349)
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EMI FILTERS BASED ON AMORPHOUS METALS

FILTRE EMI A BASE DE METAUX AMORPHES

Patent and Priority Information (Country, Number, Date):

Patent: WO 200191291 A1 20011129 (WO 0191291)

Publication Year: 2001

Claim

- 1 An electromagnetic interference filter assembly comprising:
 - (a) at least one electrical **conductor**, and
 - (b) at least one magnetic material-filled layer having opposed first and second surfaces, said at least one electrical **conductor** in close proximity to said first surface of said at least one magnetic material-filled layer.
- 4 The electromagnetic interference filter assembly as in claim 3 having a second **conductive layer** wherein the second **conductive layer** is in intimate contact with a portion of a second surface of said circuit laminate.
- 5 The electromagnetic interference filter assembly as in claim 2 wherein said circuit substrate laminate is a portion of a **printed circuit board** (PCB).
- 21 The electromagnetic interference filter assembly as in claim 3 wherein said **conductive layer** includes a material selected from the group consisting of copper, silver, aluminum. and **conductive polymer**.
- 22 The electromagnetic interference filter assembly as in claim 3 wherein said **conductive layer** is electrically grounded.
- 47 The electromagnetic interference filter as in claim 42 wherein
 - (i) said glass-coated microwires have a diameter of between about 0.5 micrometers and...
- ...as in claim 51 wherein said reinforced layer includes a reinforcing material selected from the group consisting of a glass fiber, an inorganic filler, a **polymeric** material and a combination thereof 1
54. The electromagnetic interference filter as in claim, 33 wherein said **conductive layers** includes a material selected from the group consisting of copper, silver, aluminum and **conductive polymer**.
- 55 The electromagnetic interference filter as in claim 33 having two electrical **conductors** in said each filter layer, wherein a segment of the first electrical **conductor** and a segment of the second electrical **conductor** in said each filter layer are in a plane

parallel.to the stacked filter layers.

60 The electromagnetic interference filter as in claim 33 wherein said at least one electrical **conductor** in at least one of said filter layer is winded in a meander-like pattern.

61 The electromagnetic interference filter as in claim 34 wherein a continuous electrical **conductor** formed by said **connection** of at least one electrical **conductor** in a first of said each filter layer to said at least one electrical **conductor** in a second of said each filter layer, is helically coiled around two adjacent magnetic material-filled layer.

...as in claim 84 wherein said reinforced layer includes a reinforcing material selected from the group consisting of a glass fiber, an inorganic filler, a **polymeric** material and a combination thereof.

87 The method for suppressing electromagnetic interference in functional currents as in claim 70 having two electrical **conductors** **carrying** said functional current in a differential mode.

50/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
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A direct chip attach module (DCAM).
Modul zur direkten Befestigung von Chips (DCAM).
Module d'attachement direct de puces (DCAM).
PATENT (CC, No, Kind, Date): EP 592022 A1 940413 (Basic)

...ABSTRACT A1

A low cost Surface Mount Carrier (SMC) for **carrying** integrated circuit chips mounted thereon. The carrier, or interposer, is a thin-small single layer or, a multi-layer deck of **printed circuit board** (FR-4) material with at least one direct chip attach (DCA) site for mounting a **semiconductor chip**. The DCA site has chip bonding pads wherein the integrated circuit chip's pads are **wire bonded** to or soldered to the carrier. The bonding pads are **connected** to wiring pads through interlevel vias and wiring lands or traces which may be on one of several wiring planes. The carrier is **connected** to the next level of packaging through the wiring pads. (see image in original document)

...power and said signals to said at least one integrated circuit chip, said distribution means comprised of a plurality of lands, and, at least one **layer** of a **resin** fiberglass composite material.

2. The carrier of claim 1 wherein the distribution means further comprises:
 - a plurality of **conductive** planes, said plurality of lands being located on said **conductive** planes;
 - each adjacent pair of said **conductive** planes being separated by one of said at least one layer; and, a plurality of interlevel vias.
3. The carrier of claim 2 wherein at least one of said plurality of **conductive** planes is an internal **conductive** plane.
4. The carrier of claim 3 wherein said internal **conductive** plane is a power distribution plane and/or a signal distribution plane.
5. The carrier of any of claims 1-4 wherein said at least one layer includes a plurality of **insulating layers**, each said **insulating layer** being sandwiched between a pair of said plurality of **conductive** planes.
6. The carrier of any of claims 1-5 wherein the distribution means further comprises a plurality of chip bonding pads and a plurality of carrier pads.
7. The carrier of any of claims 1-6 wherein the carrier **connection** means includes a plurality of carrier pads and a deposited solder ball on each of said plurality of carrier pads.
8. The carrier of any...

...for distributing said power and said signals to said at least one integrated circuit chip, said distribution means comprised of a plurality of carrier pads **connected** to a plurality of chip **bonding** pads by carrier **wiring** on at least one

conductive plane, said **conductive** plane being on at least one **layer** of a **resin** fiberglass composite material;
an integrated circuit chip package; and,
bonding means for mounting and **connecting** the carrier to said package.

12. The integrated circuit chip module of claim 11 wherein said at least one **conductive** plane comprises a plurality of **conductive** planes, and, each adjacent pair of said **conductive** planes being separated by one said at least one layer.
13. The integrated circuit chip module of claim 11 or 12 wherein at least two of said plurality of **conductive** planes are internal **conductive** planes and said at least one layer is a plurality of **insulating layers**, whereby each said **insulating layer** is sandwiched between a pair of said **conductive** planes.
14. The integrated circuit chip module of any of claims 11-13 wherein the chip mounting means comprises a deposited solder ball on each said chip bonding pad, whereby said deposited solder balls fixedly attach and electrically **connect** said each chip to said carrier.
encapsulant.
16. The integrated circuit chip module of any of claims 11-15 wherein said integrated circuit chip package is a leaded chip carrier with a cavity and a plurality of package **wire bond** pads, and said chip mounting means comprises: a plurality of carrier **wire bond** pads; and a **wire bond** between each of said carrier **wire bond** pads and one of said package **wire bond** pads, whereby said carrier is fixedly mounted in said cavity.
17. An integrated circuit package comprising:
a carrier, said carrier comprising:
a plurality of wiring planes,
a plurality of **insulating layers** of **resin** fiberglass composite material, each said **insulating layer** being sandwiched between an adjacent pair of said wiring planes,
a plurality of vias, each of said vias extending from a one of said wiring planes through at least one of said **insulating layers** to a second of said wiring planes,
a plurality of carrier pads, and
at least one chip mounting location on a surface of said carrier...
...package of claim 17 or 18 wherein said means for providing signal and power comprise:
a leaded chip carrier with a cavity, a plurality of **wire bond** pads, and a plurality of package leads, said carrier being fixedly mounted in said cavity; and, a plurality of **wire bonds connected** between said plurality of carrier pads and said plurality **wire bond** pads.
20. The integrated circuit package of any of claims 17-19 wherein every integrated circuit chip mounted in said at least once chip mounting
...
...is coated and protected by a deposited encapsulant.
21. The integrated circuit chip package of any of claims 17-20, wherein said carrier pads, said **wire bond** pads and said plurality

of **wire bonds** are coated and passivated by a deposited encapsulant.

22. An integrated circuit chip carrier comprising:

a leaded chip carrier with a cavity, a plurality of **wire bond** pads, and a plurality of package leads; a chip carrier comprising:

a plurality of wiring planes,
an **insulating layer** of **resin** fiberglass composite material between each adjacent pair of said wiring planes,
a plurality of vias, each of said vias extending from a first of said wiring planes through at least one of said **insulating layers** to a second of said wiring planes,
a plurality of carrier pads, and,
at least one chip mounting location having a plurality of chip power and signal pads;

51/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
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PRINTED WIRING BOARD, METHOD OF PRODUCING THE SAME AND ELECTRONIC DEVICES
LEITERPLATTE, VERFAHREN ZU DEREN HERSTELLUNG UND ELEKTRONISCHE
VORRICHTUNGEN
CARTE A CIRCUIT IMPRIME, SON PROCEDE DE PRODUCTION ET DISPOSITIFS
ELECTRONIQUES
PATENT (CC, No, Kind, Date): EP 779772 A1 970618 (Basic)
EP 779772 A1 980729
WO 9610326 960404

...ABSTRACT together into a unitary body by means of a bonding agent or thermal fusing. Formed on the surface of the insulating board (11) is a **conductor** pattern (17) that continuously runs across the fold at the cutout portion between the first portion and the second portion, and thus the **conductor** pattern assuring continuity between both sides of a printed wiring board (20) results without the need for providing through-holes. By employing such a printed wiring board, a compact and low-cost feature is implemented into **electronic apparatuses** or **portable** information **apparatuses** such as liquid crystal display devices or electronic printers, through a miniature, light-weight and flat design effort.

...CLAIMS the insulating board is provided with a cutout portion that is formed by cutting partially out the insulating board along the fold and with a **conductor** pattern that continuously extends across the fold at the cutout portion between the first portion and the second portion on the surface of the insulating...

...of the fold.

4. The printed wiring board according to claim 1, wherein said cutout portion extends over only part of the fold where the **conductor** pattern is formed.
5. The printed wiring board according to claims 3 or 4, wherein said cutout portion is made up of a plurality of...

...material or a mixture of materials or a combination of materials selected from epoxy-based resin, polyimide-based resin, BT based resin and polyester-based **resin**.

10. A multi-**layered** printed wiring board comprising a pair of outer **layers** made of **insulating** material, one or more inner **layers** made of **insulating** material sandwiched between the outer **layers**, and **conductor** patterns formed between the neighboring outer layers and inner layers, one of the outer layer having a first portion that is attached onto the neighboring...

11. A manufacturing method of a printed...

...the insulating board material along the fold that partitions the insulating board into a first portion and a second portion, forming and then patterning a **conductive film** on the surface of the insulating board to form a **conductor** pattern that

continuously extends across the fold at the cutout portion between the first portion and the second portion, and folding the insulating board along the fold with its **conductor** pattern side out, whereby the first portion and the second portion are mutually stacked.

15. A manufacturing method of a printed wiring board comprising the steps of forming a **conductive film** on the surface of an insulating board that is partitioned along a fold into a first portion and a second portion, forming a cutout portion by partly cutting out the insulating board along the fold, patterning the **conductive film** to form a **conductor** pattern that continuously extends across the fold at the cutout portion between the first portion and the second portion, and folding the insulating board along the fold with its **conductor** pattern side out, whereby the first portion and the second portion are mutually stacked.
16. The manufacturing method of a printed wiring board according to...

...the printed wiring board of claim 1.

20. The electronic apparatus according to claim 19 comprising a liquid crystal display device that is constructed by **connecting** to a liquid crystal panel a **circuit board** that is the printed wiring board of claim 1 on which a liquid crystal driving **semiconductor chip** is mounted.
21. The electronic apparatus according to claim 20 comprising as an input device a touch panel that is integrated with the liquid crystal display device.
22. The electronic apparatus according to claim 19 comprising as electronic printer means a thermal printer head that is **connected** to a **circuit board** that is the printed wiring board of claim 1 on which a driving **semiconductor chip** is mounted.

51/TI,PN,PD,PY,K/3 (Item 3 from file: 348)
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Semiconductor chip carrier and method of making it.
Halbleiterchiptrager und Verfahren zu dessen Herstellung.
Support pour puce semi-**conductrice** et procede pour sa fabrication.
PATENT (CC, No, Kind, Date): EP 359513 A2 900321 (Basic)
EP 359513 A3 901219

Semiconductor chip carrier and method of making it.
Support pour puce semi-**conductrice** et procede pour sa fabrication.

...ABSTRACT A2

A **semiconductor chip** carrier for **carrying** a single chip (15) and having a built-in capacitor, comprises a ceramic insulator body (2) having first and second opposite main faces, and a plurality of **conductor** lines (6,7) comprising power lines, ground lines and signal lines for forming **connections** to said chip extending through said ceramic body (2) from one main face to the other. A **layer** (3) of ceramic **dielectric** material is embedded in said ceramic body remote from said main faces, and **electrode layers** embedded in the ceramic body (2) contact the capacitor layer (3), to form the built-in capacitor. The power and ground lines (16) pass through and contact the capacitor layer (3) and are **connected** to said **electrodes** so that said capacitor provides capacitance between the power lines and the ground lines. To minimize noise generation and improve signal processing speed, the signal...

...CLAIMS A3

1. A ceramic **semiconductor chip** carrier for **carrying** a single chip (15) and having a built-in capacitor (3;43) providing capacitance between **conductor** lines comprising power, ground and signal lines (6,7;47,48) for the chip extending through the carrier, said capacitor being formed by at least one **dielectric layer** (4;44) and **electrodes** (5;46) embedded in the carrier, said power and ground lines (4;47) passing through said **dielectric layer** (4;44) making contact therewith and being **connected** to said **electrodes** (5;46) at the faces of the **dielectric layer** so that the capacitance is between the power lines and the ground lines, characterized in that said signal lines (7;48) extend past the **dielectric layer** (4;44) without contacting it at locations spaced laterally from it.
2. A **semiconductor chip** carrier according to claim 1 having a ceramic insulator body (2;42) in which said capacitor layer (4;44) of ceramic dielectric material is embedded remote from opposed main faces of said body (2), the **electrodes** (5) being **electrode layers** embedded in said ceramic body (2) and contacting said capacitor layer (4).
3. A **semiconductor chip** carrier according to claim 1 or claim 2 wherein each said signal line (7;48) is spaced laterally from said **dielectric layer** (4;44) by not less than 50 (mu)m.
4. A **semiconductor chip** carrier according to claim 3

wherein each said signal line (7;48) is spaced laterally from said **dielectric layer** (4;44) by not less than 100 (mu)m.

5. A **semiconductor chip** carrier according to any one of claims 1 to 4 wherein there is a single said capacitor layer(4;44).
6. A **semiconductor chip** carrier according to claim 5 wherein there are two said **electrodes** (5;46) only, respectively on opposite faces of said single capacitor layer (4;44).
7. A **semiconductor chip** carrier according to any one of claims 1 to 6 wherein each said **conductor** line (6,7;47,48) extends substantially straight through said carrier from one main face thereof to the opposite main face thereof.
8. A **semiconductor chip** carrier according to any one of claims 1 to 7 wherein the power and ground lines (6;47) on the one hand and the signal...
14. A **semiconductor chip** carrier according to any one of claims 1 to 13 having a ceramic insulator body (2) of ceramic glass and sintered barrier layers (45) on each face of said **dielectric layer** (4) to prevent diffusion of components of the **dielectric layer** (4) into the ceramic glass during firing of the **chip** carrier.
15. A **semiconductor chip** carrier according to any one of claims 1 to 14 having a single **semiconductor chip** (15) mounted thereon and **connected** to said **conductor lines**(6,7;47,48).
16. A **semiconductor chip** carrier and **chip** according to claim 15 wherein said chip (15) is mounted on said carrier by solder elements (18) which make direct **connection** between **electrodes** of the chip and said **conductor** lines (6,7;47,48) at one main face of the carrier.
17. A **semiconductor chip** carrier and **chip** according to claim 15 or claim 16 wherein said chip (15) is hermetically enclosed by a ceramic housing (16) sealed to said **chip** carrier.

...larger area than said at least one green sheet (10;44) of dielectric material, such that on assembly and firing of said green sheets some **conductor** lines formed do not pass through said capacitor **layer** and other **conductor** lines formed do pass through said capacitor layer, said green sheets further **carrying electrode-forming material** (14;46) for forming **electrodes** adjacent said capacitor **layer** and contacting said **conductor** lines which do pass through said capacitor layer.

27. A combination of green sheets according to claim 26 wherein there are more than two said green sheets (8;42) of insulator material and two of said sheets of insulator material **carry** said **electrode-forming material**.
28. A combination of green sheets according to claim 26 further comprising at least two intermediate sheets (45) of composition different from that...

09/26/2002 09/939,457

51/TI,PN,PD,PY,K/4 (Item 1 from file: 349)
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EMI FILTERS BASED ON AMORPHOUS METALS

FILTRE EMI A BASE DE METAUX AMORPHES

Patent and Priority Information (Country, Number, Date):

Patent: WO 200191291 A1 20011129 (WO 0191291)

Publication Year: 2001

4 The electromagnetic interference filter assembly as in claim 3 having a second **conductive layer** wherein the second **conductive layer** is in intimate contact with a portion of a second surface of said circuit laminate.

5 The electromagnetic interference filter assembly as in claim 2 wherein said circuit substrate laminate is a portion of a **printed circuit board** (PCB).

21 The electromagnetic interference filter assembly as in claim 3 wherein said **conductive layer** includes a material selected from the group consisting of copper, silver, aluminum. and **conductive polymer**.

22 The electromagnetic interference filter assembly as in claim 3 wherein said **conductive layer** is electrically grounded.

23 The electromagnetic interference filter assembly as in claim 1 having two electrical **conductors** wherein a segment of the second electrical **conductor** and a segment of the first electrical **conductor** are in a plane parallel to said at least one magnetic material-filled layer.

24 The electromagnetic interference filter assembly as in claim 23 wherein a spacing between said two electrical **conductors** is between about 2 mil. and about 1 00 mil.

19
. The electromagnetic interference filter assembly as in claim 2 having two electrical **conductors** wherein said two electrical **conductors** are supported by two opposite surfaces of said circuit substrate laminate.

26 The electromagnetic interference filter assembly as in claim 3 having a first and a second magnetic material-filled layer, said **circuit** substrate laminate is **sandwiched** between respective inner surfaces of said first and second magnetic material-filled layer.

27 The electromagnetic interference filter assembly as in claim 26 having a second **conductive layer**, said second **conductive layers** in intimate contact with an outer surface of said second magnetic material-filled layer.

28 The electromagnetic interference filter assembly as in claim 27 wherein said two **conductive layers** are electrically **connected** via through-holes in said circuit substrate laminate.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/26/2002 09/939,457

47 The electromagnetic interference filter as in claim 42 wherein
(i) said glass-coated microwires have a diameter of between about 0.5
micrometers and...

...as in claim 51 wherein said reinforced layer includes a reinforcing
material selected from the group consisting of a glass fiber, an
inorganic filler, a **polymeric** material and a combination thereof 1
5 54. The electromagnetic interference filter as in claim, 33 wherein
said **conductive layers** includes a material selected from the
group consisting of copper, silver, aluminum and **conductive**
polymer.

55 The electromagnetic interference filter as in claim 33 having two
electrical **conductors** in said each filter layer, wherein a segment
of the first electrical **conductor** and a segment of the second
electrical **conductor** in said each filter layer are in a plane
parallel.to the stacked filter layers.

09/26/2002 09/939,457

53/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
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WIRING METHOD AND WIRING DEVICE
VERFAHREN UND VORRICHTUNG ZUR VERDRAHTUNG
PROCEDE DE CABLAGE ET DISPOSITIF DE CABLAGE
PATENT (CC, No, Kind, Date): EP 1100296 A1 010516 (Basic)
WO 200069234 001116

...ABSTRACT A1

A wiring method is provided, in which a wire **conductor** is stuck on a surface of a substrate by causing a three-dimensional relative movement between a wiring head (2) for guiding the wire **conductor** (5) and the substrate (11) such that the wiring head relatively moves along an **adhesive layer** (12) on the surface of the substrate and the wiring head and the **adhesive layer** intermittently come close to each other for point contact. A wiring **apparatus** for **carrying** out the wiring method includes a table (1) for supporting the substrate, a wiring head arranged for reciprocating motion between a close position in which the wiring head can be in point contact with the **adhesive layer** and a distant position in which the wiring head is most distant from the **adhesive layer**, and a moving mechanism (3) for causing a translational motion of the wiring head along the surface of the substrate under the control of a control section (4). The wire **conductor** is stuck onto the surface of substrate point by point, to be laid thereon, whereby a planar transformer, an antenna coil or a **conductor** pattern is formed on the substrate.

...CLAIMS A1

1. A wiring method comprising the steps of:
 - (a) forming an **adhesive layer** on a surface of a substrate:
and
 - (b) sticking a wire **conductor** on the surface of the substrate by causing a three-dimensional relative movement between the substrate and a wiring head adapted to guide the wire **conductor** such that the wiring head relatively moves along the **adhesive layer** formed on the surface of the substrate and the wiring head and the **adhesive layer** intermittently come close to each other for point contact.
substrate executed in said step (b).
4. A wiring method according to claim 1, further comprising the steps of:
 - (c) providing a second **adhesive layer** on the wire **conductor** stuck on the surface of the substrate; and
 - (d) sticking a second wire **conductor** on the second **adhesive layer** by causing a three-dimensional relative movement between the substrate and the wiring head adapted to guide the second wire **conductor**, such that the wiring head relatively moves along the second **adhesive layer** and the wiring head and the second **adhesive layer** intermittently come close to each other for point contact.
5. A wiring method according to claim 4, wherein:
the three-dimensional relative movement between the...

- ...and the substrate executed in said step (b) includes a relative translational motion between the wiring head and the substrate which is performed along the **adhesive layer**, and a relative reciprocal motion between the wiring head and the substrate which is performed in a direction of thickness of the substrate, the relative translational motion being executed in accordance with a first two-dimensional pattern, so that a first wire-**conductor** pattern corresponding to the first two-dimensional pattern is formed on the surface of the substrate;
- in said step (c), the second **adhesive layer** is formed on the first wire-**conductor** pattern; and
- in said step (d), a relative translational motion between the substrate and the wiring head adapted to guide the second wire **conductor** is executed in accordance with a second two-dimensional pattern, so that a second wire-**conductor** pattern corresponding to the second two-dimensional pattern is formed on the second **adhesive layer**.
6. A wiring method according to claim 4, wherein in said step (c), an adhesive sheet is stuck on the first wire-**conductor** pattern to form the second **adhesive layer**.
7. A wiring method according to claim 4, wherein **conductors** with an **insulating coating** are used as the wire **conductor** and the second wire **conductor**.
8. A wiring apparatus, comprising:
- a supporting mechanism for supporting a substrate having a surface thereof provided with an **adhesive layer**;
 - a wiring head for guiding a wire **conductor**, said wiring head being arranged for reciprocal motion between a close position in which said wiring head can be in point contact with said **adhesive layer** formed on the surface of the substrate and a distant position in which said wiring head is most distant from the **adhesive layer**;
 - a moving mechanism for causing a relative translational motion between said wiring head and said substrate such that said wiring head relatively moves along the...
16. An IC card manufacturing method comprising the steps of:
- (a) sticking an electrical component on an adhesive sheet;
 - (b) laying a wire **conductor** on said adhesive sheet by causing a relative movement between said **adhesive layer** and a wiring head adapted to guide said wire **conductor** such that said wiring head relatively moves along a surface of said adhesive sheet and said wiring head and said adhesive sheet intermittently come close to each other for point contact;
 - (c) electrically **connecting** each end of said wire **conductor** to said electrical component;

09/26/2002 09/939,457

53/TI,PN,PD,PY,K/2 (Item 2 from file: 348)
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Wafer-scale assembly of chip-size packages
Scheibebereichsanordnung von Packungen in Chip-Grosse
Assemblage a l'echelle d'une gallette d'empaquetages a largeur de puce
PATENT (CC, No, Kind, Date): EP 955676 A2 991110 (Basic)
EP 955676 A3 000510

...ABSTRACT including a plurality of circuits is provided with a plurality of metal contact pads as electrical entry and exit ports. A first wafer-scale patterned **polymer** film **carrying** solder balls for each of the contact pads on the wafer is positioned opposite the wafer, and the wafer and the film are aligned. The...

...the wafer to the surface of the wafer and into the solder balls, which reflow onto the contact pads, while the thermal stretching of the **polymer** film is mechanically compensated. The uniformity of the height of the liquid solder balls is controlled either by mechanical stoppers or by the precision linear motion of motors. After cooling, the solder balls solidify and the first **polymer** film is removed. The process is repeated for assembling sequentially a wafer-scale patterned interposer overlying all of the solder balls and the wafer and contacting each solder ball with a soldered joint, and a second wafer-scale patterned film **carrying** solder balls contacting the interposer. In each process, the wafer is heated uniformly and rapidly and without moving it, the alignment is maintained during heating by mechanically compensating for the thermal stretching of the **polymer** film, and the uniformity of the height of the liquid solder balls is controlled by mechanical stoppers or position closed-loop linear actuators. The second ...

...CLAIMS wherein said support is a semiconductor wafer integral with said circuits.

3. The assembly according to Claim 1 wherein said support is a substrate with **semiconductor chips** attached.

4. The **semiconductor** assembly according to Claim 2 or Claim 3 wherein said semiconductor assembly can be readily separated into discrete chips.

5. An assembly comprising:
an interposer of electrically insulating material having electrically **conductive** paths extending through said interposer from one surface to an opposite surface, forming electrical entry and exit ports on said insulating interposer;
at least one...

...that each of said contact pads is contacted by one of said solder balls;

an interposer of electrically insulating and mechanically elastic material having electrically **conductive** paths extending through said interposer from one surface to the opposite surface forming electrical entry and exit ports on said insulating interposer;
a second planar...

...balls attached to plastic films.

15. The apparatus according to any of Claims 9 to 14 wherein said metallic entities are a multitude of electrically **conductive** fibers extending through an electrically non-**conductive layer** from one surface to the opposite surface, while remaining insulated from adjacent fibers.
16. The apparatus according to any of Claims 9 to 15 wherein...

...apparatus according to any of Claims 9 to 18 wherein said metallic entities attached to plastic films are metal ports of interposers made of electrically **conductive** paths from one surface to the opposite surface of a **layer** made of electrically **insulating** material.

20. The apparatus according to any of Claims 14 to 19 wherein each of said solder balls is aligned with one of said metal method according to Claim 23 or Claim 24 wherein said support is a substrate with **semiconductor chips** attached.

26. The method according to any of Claims 23 to 25 wherein said forming of said array of solder balls comprises:
providing a **polymer** film having a plurality of discrete adhesive areas;
providing a plurality of solder balls, one of said solder balls being placed on each of said **adhesive** areas;
aligning said **film** with the circuit surfaces of said integrated circuits on said support so that each of said solder balls is placed into alignment with one of...

...said radiant energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said contact pads; and removing said **polymer** film.

27. The method according to any of Claims 21 to 26 wherein said semiconductor assembly is fabricated in a controlled environment.
28. The method...

09/26/2002 09/939,457

53/TI,PN,PD,PY,K/3 (Item 3 from file: 348)
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Method for coating an electronic component and device for **carrying**
out the method
Verfahren zur Umhüllung eines elektronischen Bauelements und Vorrichtung
zur Ausführung des Verfahrens
Procede d'enrobage d'un composant electronique et dispositif de mise en
oeuvre dudit procede
PATENT (CC, No, Kind, Date): EP 741369 A1 961106 (Basic)
EP 741369 B1 020703

Method for coating an electronic component and device for **carrying**
out the method

...ABSTRACT Translated)

Coating an electronic component for protection

A semiconductor component (11) is located on an **insulating film** (20). It has perforations (21,22) around it's periphery for **connections** (12) between the semiconductor and electrical contacts (30) on the lower side of the **insulating film** (20). After forming the perforations (21,22), locating the semiconductor (11), and making the **connections** (12) a drop of liquid resin (13) is used to seal the unit and protect it against mechanical or chemical damage.

The resin used is thermohardening and of low viscosity. It's size is precalibrated so, with the effect of surface tension, it covers the semiconductor (11) and the adjacent **connections** (21,22).

...ABSTRACT A1

Coating an electronic component for protection

A semiconductor component (11) is located on an **insulating film** (20). It has perforations (21,22) around it's periphery for **connections** (12) between the semiconductor and electrical contacts (30) on the lower side of the **insulating film** (20). After forming the perforations (21,22), locating the semiconductor (11), and making the **connections** (12) a drop of liquid resin (13) is used to seal the unit and protect it against mechanical or chemical damage.

The resin used is thermohardening and of low viscosity. It's size is precalibrated so, with the effect of surface tension, it covers the semiconductor (11) and the adjacent **connections** (21,22)

1. A method of coating an electronic component (10; 10') comprising at least one **semiconductor chip** (11; 11') placed on an **insulating film** (20; 20') **carrying** electric contacts (30; 30') to which said **semiconductor chip** is **connected** by **connection** wires (12; 12') passing through holes (21; 21') formed in said **insulating film** (20; 20'), the said method comprising the following steps:
 - making said holes (21, 21') in the **insulating film** (20; 20') around a zone (Z; Z') for receiving the **semiconductor chip** (11; 11'),
 - placing the **semiconductor chip** on the **insulating film** in said zone (Z; Z'),

- connecting said **connection** wires (12; 12') between the **semiconductor chip** (11; 11') and the electric contacts (30; 30') through the holes (21; 21'),
- depositing a drop of resin (13; 13') on the **semiconductor chip** and on the **connection** wires, wherein the spreading of the drop (13; 13') is restricted and even controlled by the surface tension forces created on the said drop (13...
...defined solely by the holes (21, 22; 21', 22')).
- 2. A coating method according to claim 1, wherein the said resin is a liquid thermosetting **resin**.
- 3. A **coating** method according to claim 2, wherein a low viscosity resin, e.g. epoxy or acrylic, is used.
- 4. A coating method according to claim 1...
- ...said holes (21).
- 5. A coating method according to claim (4) wherein the supernumerary holes (22) are made around the zone (Z) for receiving the **semiconductor chip** (11).
- 6. A coating method according to claim 1 or 2, wherein said **semiconductor chip** (11') is placed in a window (22') formed in the **insulating film** (20'), and said holes are located outside said window (22').
- 7. Apparatus for implementing the coating method according to any of claims 1 to 6, comprising:
 - a dispenser (D) suitable for delivering volume-calibrated drops of resin via a flexible feed hose (T), and
 - a coating head (40) **connected** to the dispenser (D) by said flexible feed hose (T), and including a coating chamber (41) suitable for receiving said drops of volume-calibrated **resin**, said **coating** chamber (41) having an outline (C; C') designed to cover said holes at least in part (21, 22; 21', 22')....
- ...CLAIMS B1
- 1. Procédé d'enrobage d'un composant électronique (10 ; 10') comprenant au moins une pastille semi-**conductrice** (11 ; 11') disposée sur un film isolant (20 ; 20') portant des contacts électriques (30 ; 30') auxquels ladite pastille semi-**conductrice** est reliée par des fils (12 ; 12') de connexion passant à travers des perforations (21 ; 21') ménagées dans ledit film isolant (20 ; 20'), ledit procédé
...

53/TI,PN,PD,PY,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor device comprising a package.
Halbleiteranordnung mit einer Packung.
Dispositif semi-**conducteur** comprenant un empaquetage.
PATENT (CC, No, Kind, Date): EP 562629 A2 930929 (Basic)
EP 562629 A3 940309

Dispositif semi-**conducteur** comprenant un empaquetage.

...ABSTRACT be used for a variety of different purposes in a flexible manner, and which is suitable for automatic assembly. It has a metal board (1) **carrying** a **semiconductor** device **chip** (6) on the central part thereof. An **insulating layer** (2), a ceramic laminated wiring board (3), an organic film (4), and a lead frame (5) are laminated one on another on the metal board so as to surround the **semiconductor** device **chip**. The lead frame is **connected** to the **semiconductor** device **chip** through the ceramic laminated wiring board. The assembly thus formed is sealed with a synthetic resin. (see image in original document)

...CLAIMS A3

1. A semiconductor device comprising a metal board, a **semiconductor** device **chip** mounted on said metal board, a ceramic laminated wiring board having wiring layers and mounted on said metal board so as to surround said **semiconductor** device **chip**, and a lead frame bonded to said ceramic laminated wiring board through an **insulating layer**, said **semiconductor** device **chip**, said ceramic laminated wiring board and said lead frame having their inner portions sealed with a synthetic resin.
2. A semiconductor device comprising a ceramic...

- ...or between its layers and/or on its back, a lead frame having a plurality of leads and bonded to said wiring board through an **insulating adhesive layer**, and a **semiconductor** device **chip** mounted on said device chip mounting portion of said wiring board, at least some of the leads of said lead frame being electrically **connected** to said **semiconductor** device **chip** through said wiring layer of said ceramic laminated wiring board, said **semiconductor** device **chip**, said ceramic laminated wiring board and said lead frame having inner portions thereof sealed with a resin.
3. A semiconductor device as claimed in claim 2 wherein said ceramic laminated wiring board comprises a ceramic board made mainly of aluminum nitride and **carrying** said **semiconductor** device **chip** in the center thereof, and at least two wiring layers and at least one **insulating layer** which are laminated so as to alternate with each other on said ceramic board.
 4. A semiconductor device as claimed in any of claims 1 - 3 wherein said **insulating layer** is formed with via holes filled with a

conductive material at portions right under some of the leads of said lead frame, some of said leads being electrically **connected** to said wiring layer of said wiring board through the **conductive** material in said via holes.

9. A semiconductor device as claimed in any of claims 1 - 6 wherein two separate wiring layers...

...chip mounting portion and the other wiring layer covering said intermediate portion, and wherein said lead frame is bonded to said outermost portion through said **insulating adhesive layer**, the leads of said lead frame being electrically **connected** to said **semiconductor device chip** through the wiring layer provided on said intermediate portion, the wiring layer provided on the outermost portion being electrically **connected** to a power source lead or a grounding lead.

10. A semiconductor device comprising a ceramic wiring board having on its surface a device chip...

...corresponding to the respective leads of said lead frame, and having substantially the same shape as the inner portion of the respective leads, and a **semiconductor device chip** mounted on said device chip mounting portion, the leads of said lead frame being electrically **connected** to the **semiconductor device chip** through the wiring layers of said wiring board, said **semiconductor device chip**, said ceramic wiring board and said lead frame having inner portions sealed with a resin.

11. A semiconductor device as claimed in any of claims...

...alloy.

13. A Semiconductor device as claimed in any of claims 1 - 12 wherein some of the wiring layers of said wiring board are electrically **connected** together through **via-connection**.

14. A semiconductor device as claimed in any of claims 1 - 13 wherein at least one of the **insulating layers** between the wiring layers are provided with cutouts, whereby the wiring layers on both sides of said **insulating layer** are directly

09/26/2002 09/939,457

53/TI,PN,PD,PY,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Method of forming a planarized thin film surface covered wire bonded
semiconductor package
Herstellungsverfahren einer Halbleiterpackung mit Drahten und eine
Oberfläche mit planarisierter Dunnfilmdecke
Methode de fabrication d'un empaquetage semi-conducteur comprenant
des fils et une surface couverte d'un film mince egalise
PATENT (CC, No, Kind, Date): EP 513521 A2 921119 (Basic)
EP 513521 A3 930714
EP 513521 B1 990630

...ABSTRACT A2

This is a **semiconductor chip** (12) in which the
conductive path between the chip and the lead frame (14) via wires
(16) can be easily and reproduceably improved. This is accomplished by
improving the bond...

...its respective lead even if the bonded contact breaks or fails at or
immediately adjacent to the bonding point.

This is accomplished by placing an **insulating layer** (11b)
on the active surface of each chip, **carrying** input and output
bonding pads thereon, to which lead frame **conductors** have been
connected by bonding wires. The **insulating layer** is a
thermosetting **adhesive** (17) and is placed over the lead frame, the
bonding wires and the active face of the **semiconductor chip**
so that when a lamination force is applied to the **insulating**
layer the wires will be crushed and held against their respective
pads and against the respective leads to which they are **connected**
and the active face of the semiconductor protected by the adhesive
bonding thereto. In this way greater contact between the wires and the
leads is...

CLAIMS 1. Method of forming a semiconductor package comprising the steps
of:

- a) providing a **semiconductor chip** (12; 52) having first and
second major surfaces with input and output bonding pads on said
first major surface;
- b) providing a lead frame (10...

...plurality of leads (14; 51, 51a, 51b);

- c) bonding said plurality of said leads (14; 51, 51a, 51b) on said first
major surface of said **semiconductor chip** (12; 52) via an
insulating layer (11, 55);
- d) **connecting** respective ones of said plurality of leads (14; 51,
51a, 51b) to respective ones of input and output bonding pads by
conductive bonding wires (16; 59) therebetween;
- e) placing an **insulating film** (17, 18 ; 57) over the
connected plurality of leads (14; 51, 51a, 51b) of said lead
frame (10; 50), said first major surface of said **semiconductor**
chip (12; 52) and said **conductive** bonding wires (16; 59)
with said **insulating film** (17; 18; 57) abutting said

plurality of leads (14; 51, 51a, 51b) and said **conductive** bonding wires (16; 59),

- f) applying heat and force to said **insulating film** (17; 18; 57) sufficient to force said **conductive** bonding wires (16; 59) against the respective one of input and output bonding pads and the respective ones of said plurality of leads (14; 51, 51a, 51b) to which they are bonded and sufficient to force material of said **insulating film** (17; 18; 57) between said plurality of leads (14; 51, 51a, 51b); characterized in that

said **insulating film** (18; 57) is a polyimide film (18) with a thermosetting acrylic **layer** (17) thereon, said **insulating film** (18, 57) is equal in size to said **semiconductor chip**, and the placing step e) comprises aligning said **insulating film** (17, 18; 57) to said **semiconductor chip** (12; 52) with said thermosetting **adhesive layer** (17) facing said **semiconductor chip** (12; 52);

- g) the heat and force applied in step f), the force of which is applied by a heated platen which causes said thermosetting acrylic **adhesive layer** (17) to soften or melt and to be forced between said plurality of leads (14; 51, 51a, 51b) and around said **conductive** bonding wires (16; 59); and
- h) the assembly obtained after step g) is heated to cure said thermosetting adhesive.
2. Method according to claim 1, characterized in that the **insulating film** (18; 57) is a polyimide **film** and said **adhesive layer** is a B-stage thermoset adhesive.
3. Method according to anyone of claims 1 or 2, characterized in that the thermosetting acrylic **adhesive layer** ranges in thickness between 76.2 (μ m) and 254(μ)m (3 and 10 mils).
4. Method according to anyone of claims 1 to 3, characterized in that steps a to c is accomplished by securing said **insulating layer** (11; 55) on said first major surface of the **semiconductor chip** (12; 52), and securing said lead frame (10; 50) on said **insulating layer** (11; 55).

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53/TI,PN,PD,PY,K/6 (Item 6 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

COMPONENTS WITH RELEASABLE LEADS

COMPOSANTS DOTES DE FILS DETACHABLES

Patent and Priority Information (Country, Number, Date):

Patent: WO 9940761 A1 19990812

Publication Year: 1999

Fulltext Availability:

Claims

English Abstract

A microelectronic component is made by providing a starting structure having a **dielectric layer** (22) and leads on a surface of the **dielectric layer**. The **dielectric layer** is etched to partially detach the leads (24) from the **dielectric layer**, leaving a portion of each lead releasably **connected** to the **dielectric layer**. Ends of the leads (24) may be **connected** to contacts (52) on a microelectronic element (50), such as the contacts on a **semiconductor chip** or wafer, before the **dielectric layer** (22) is etched to partially detach the leads (24) from the **dielectric layer**. The lead is partially detached from the **dielectric layer** so that the **dielectric layer** can be broken or peeled away from the leads during the step of moving the microelectronic element (50) and **dielectric layer** (22) away from one another.

Claim

INDUSTRIAL APPLICABILITY

The industrial applicability of the invention is in manufacturing microelectronics.

CLAIMS:

1 A method of making a **connection** component comprising the steps of

(a) providing a starting structure including one or more metallic leads overlying a **dielectric layer**; and

(b) etching portions of said **dielectric layer** disposed beneath

said one or more leads by contacting said starting structure with an etchant so as to leave one or more parts of one or more said leads **connected** to said **dielectric layer** by etch-defined **connection** regions smaller than such parts.

2 A method as claimed in claim 1 wherein said leads overlie a first surface of said **dielectric layer** and wherein said etching step includes the step of exposing said first surface, with said leads thereon, to said etchant.

3 A method as claimed in claim 1 wherein said etching step is perforined so as to leave said leads **connected** to said **dielectric layer** by anchor regions adjacent first ends of the

leads and by said etch-defined **connection** region adjacent second ends of the leads.

4 A method as claimed in claim 3 wherein said etching step is performed so as to remove dielectric material from beneath an elongated region of each said lead between said anchor region and said etch-defined **connection** region and thereby at least partially detach the elongated region of each said lead from said **dielectric layer**.

5 A method as claimed in claim 4 wherein said etching step is performed so as to entirely detach the elongated regions of said leads from said **dielectric layer** over at least part of the lengths thereof.

6 A method as claimed in claim 4 wherein said etching step is performed so as to leave an elongated, web-like **polymeric connecting** region extending lengthwise along the elongated region of each said lead and extending vertically between the lead and the etched surface of the **dielectric layer**.

7 A method as claimed in claim 3 wherein said etching step is performed so as to etch said **dielectric layer** beneath said anchor regions.

8 A method as claimed in claim 7 wherein said etching of said **dielectric layer** beneath said anchor regions leaves **polymeric** anchor **connecting** elements **connecting** said anchor regions of said leads to said **polymeric** layer.

9 A method as claimed in claim 3 further comprising the step of providing a mask over a part of said **dielectric layer** adjacent the first ends of said leads during so that said mask is present during said etching step, so that said mask inhibits etching of...

...regions.

10 A method as claimed in claim 2 further comprising the step of providing a mask over said first surface in a part of **dielectric layer** so that said mask is present during said etching step and said mask inhibits etching of said **dielectric layer** in said part thereof.

11 A method as claimed in claim 10 wherein said mask overlies portions of said leads disposed on said part of said **dielectric layer**.

12 A method as claimed in claim 11 wherein said mask is attached to said **dielectric layer** and supported by said **dielectric layer**.

13 A method as claimed in claim 2 wherein said etching step 11 includes the step of contacting the **dielectric layer** with a gaseous etchant.

62/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Method and device for encapsulation of three-dimensional semi-
conductor chips
Verfahren und Vorrichtung zur Verkapselung von dreidimensionalen
Halbleiterplattchen
Procede et dispositif d'encapsulation en trois dimensions de pastilles
semi-conductrices
PATENT (CC, No, Kind, Date): EP 565391 A1 931013 (Basic)
EP 565391 B1 981104

- CLAIMS 1. Method of interconnection of **semiconductor chips** (1),
each having a lower face, an upper face opposite the lower face, and
four sides, and including connection pads (15), the method
comprising, in succession, the following steps:
- a first step of extending the pads (15) of each chip with the aid
of connection means comprising **conductive** tracks (41, 31)
placed on an **insulating film** (2), the tracks being
connected to the pads with the aid of **conductors** (16, 17, 18);
- a second step of stacking (70) the chips (1) and fastening of the
latter and of the **conductors** in an electrically insulating
material (7), so that the **conductors** are flush with the side
faces of the stack;
- a third step of forming electrical connections (C) between the
conductors, on the side faces of the stack; the method being
characterized in that:
- during the first step, the tracks are connected to the pads on at
most three sides (12, 13, 14) of the chip;
- during the second step, the **conductors** are flush with the
side faces of the stack except for at least the side face (71),
called the fourth side face, located on the...
...being connected to heat dissipation means.
2. Method according to Claim 1, characterized in that the connection
means are formed, for each chip, by the **conductors** and the
insulating film (2), the latter having a frame (3) and a
central part (4), the latter having a surface area similar to that of
the chip, the...
...consisting in placing the chip in line with the central part, in
connecting the pads (15) of each chip, each, with the aid of a
conductor (16), to a **conductive** track (31) located on one
of the three sides of the frame, these three sides being located
opposite the said three sides (12, 13, 14) of the chip and the pads
(15) located on the fourth side (11) of the chip (1) being connected,
each with the aid of a **conductor** (17), to a **conductive**
track (41) carried by the central part and then, with the aid of
another **conductor** (18), to a **conductive** track (31)
carried by one of the three sides of the frame.
3. Method according to Claim 2, characterized in that the central part
(4) has **dimensions** which are **smaller** than those of the
chip (1) and that it is placed on that face of the chip which carries

its pads (15).

4. Method according...

...which are greater than those of the chip (1) and that it is placed on that rear face (19) of the chip which does not **carry** its pads (15).

5. Method according to one of Claims 2 to 4, characterized in that the central part is of the multilayer type, having a plurality of electrically **conductive layers** separated by **insulating layers**.

6. Method according to one of Claims 2 to 5, characterized in that, during the second step, the stack (70) is furthermore cut (ZZ) between...

...one of the preceding claims, characterized in that the third step is divided into two sub-steps:

- the first sub-step consisting in depositing a **conductive layer** over all the faces of the stack (70);

- the second sub-step consisting in laser-etching the **conductive layer** in order to form electrical connections (C) connecting the **conductors** (F) together.

9. Method according to one of Claims 1 to 7, characterized in that the third step is divided into the following sub-steps:

- formation of grooves in the stack in the region where the **conductors** are flush and in the desired pattern for the connections (C);

11. Device for the encapsulation of **semiconductor chips** (1), each having a lower face, an upper face opposite the lower face, and four sides, and including connection pads (15), the device comprising connection means for each of the chips, these connection means comprising **conductive** tracks placed on an **insulating film** (2), the said **conductive** tracks being connected to the pads with the aid of **conductors** and providing the extension of the pads (15) of the chips on the sides of these chips, the chips and their connection means being fastened to each other with the aid of an electrically insulating material (7) in order to form a stack (70), so that the **conductors** are flush with the side faces of the stack, and so that the **conductors** are connected together electrically by connections (C) made on the side faces of the stack, the device being characterized in that the connection means provide the extension of the pads of the chips on at most three sides (12, 13, 14) of the chips, in that the **conductors** are flush with the side faces of the stack except for at least the side face (71), called the fourth side face, located on the...Claim 11, characterized in that the said face (71) of the stack which is located on the fourth side of the chips does not have **conductors** (F), that the stack furthermore includes stack pads (81) formed on one or more of its faces except for the said side face (71), these stack pads being intended for connecting the stack to external circuits, and in that the connections (C) furthermore connect at least some of the **conductors** to the stack pads.

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70/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor device

Halbleiteranordnung

Dispositif semiconducteur

PATENT (CC, No, Kind, Date): EP 1069615 A2 010117 (Basic)

EP 1069615 A3 020403

...ABSTRACT A2

Interconnection wiring lines (30) connecting electrode terminals (16) with external connection terminals (12) are provided for **semiconductor chips** with a large number or high density of external connection terminals. A semiconductor device is disclosed which includes a **semiconductor chip (10)** having **electrode terminals (16)** electrically connected to external connection terminals (12). The **semiconductor chip (10)** has an **electrode terminal carrying surface (11)** including the **electrode terminals (16)** and **interconnection wiring lines (30)**. Each of the **interconnection wiring lines (30)** have one end bonded to one of the **electrode terminals (16)** and the other end forming a pad (30a). An **insulating layer (34)** is formed over the **electrode terminal carrying surface (11)** to cover the **electrode terminals (16)**, the **interconnection wiring lines (30)** and the remaining area of the **electrode terminal carrying surface (11)**. **Conductor lands (32)** are formed on the **insulating layer (34)**, each of the **conductor lands (32)** having a part forming a via (36) extending through the **insulating layer (34)** to the pad (30a) of one of the **interconnection wiring lines (30)**. The external **connection terminals (12)** are formed on the lands (32).

CLAIMS 1. A semiconductor device including a **semiconductor chip (10)** having **electrode terminals (16)** electrically connected to external connection terminals (12), the **semiconductor device chip (10)** having an **electrode terminal carrying surface (11)** including the **electrode terminals (16)** and **interconnection wiring lines (30)**, each of the **interconnection wiring lines (30)** having one end bonded to one of the **electrode terminals (16)** and the other end forming a pad (30a);
an **insulating layer (34)** formed over the **electrode terminal carrying surface (11)** to cover the **electrode terminals (16)**, the **interconnection wiring lines (30)** and the remaining area of the **electrode terminal carrying surface (11)**;
conductor lands (32) formed on the **insulating layer (34)**, each of the **conductor lands (32)** having a part forming a via (36) extending through the **insulating layer (34)** to the pad (30a) of one of the **interconnection wiring lines (30)**; and
the external connection terminals (12) formed on the lands (32).
2. A semiconductor device according to claim 1, wherein the lands (32)

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

are...

...in diameter than the pads (30a)

3. A semiconductor device according to claim 1 or claim 2, wherein the via (36) is formed of a **conductor layer** (44) **coating** a side wall and a bottom of a through hole (34a) penetrating the **insulating layer** (34), the bottom of the through hole (34a) being defined by a surface of an **interconnection wiring line** (30).
4. A semiconductor device according to any one of the preceding claims, wherein the lands (32) occupy areas of the **insulating layer** (34) that overlap areas of the **electrode** terminal **carrying** surface (11) that are occupied by the **interconnection wiring lines** (30).

71/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Process for the fabrication of an interconnection level in a
semiconductor chip having an antifuse
Verfahren zum Herstellen einer Verdrahtungsebene auf einem Halbleiterchip
mit einer Antifuse
Procede pour la fabrication d'un niveau d'interconnexion dans une puce
semiconductrice avec antifusible
PATENT (CC, No, Kind, Date): EP 1148542 A2 011024 (Basic)

...ABSTRACT Translated)

Production of **conducting** pathways on an integrated chip comprises
applying a stacked **dielectric layer**, **carrying out**
photolithography, etching, applying **conducting** material and
removing, and applying an **insulating layer**

Production of **conducting** pathways on an integrated chip
comprises:

- (i) applying a stacked **dielectric layer**;
- (ii) **carrying out** photolithography to define contact holes (30);
- (iii) etching the holes;
- (iv) applying **conducting** material and removing outside of the
holes;
- (v) applying an **insulating layer** (50);
- (vi) **carrying out** photolithography to define **conducting**
pathways;
- (vii) etching **conducting** pathway trenches (80); and
- (viii) applying **conducting** material and removing outside of the
trenches.

Production of **conducting** pathways on an integrated chip
comprises:

- (a) applying a stacked **dielectric layer** consisting of a
lower (21) and an upper **dielectric layer** (22) with an
antireflection layer (60) arranged between them;
- (b) **carrying out** photolithography to define contact holes (30) in
the **dielectric layer**;
- (c) etching the holes in the stacked **layer**;
- (d) applying **conducting** material and removing the material
outside of the holes so that recesses (40) are formed over the contact
holes;
- (e) applying an **insulating layer** (50);
- (f) **carrying out** photolithography to define **conducting**
pathways in the region of individual contact holes on the
insulating layer;
- (g) etching **conducting** pathway trenches (80) in the
insulating layer and the upper **dielectric layer**
lying underneath so that the antireflection layer acts as an etch stop;
and
- (h) applying **conducting** material and removing the material
outside of the trenches and the recesses over the contact holes.

Preferred Features: The **insulating layer** is made from
silicon nitride. The antireflection layer is a light-absorbing inorganic
material, especially silicon oxynitride.

71/TI,PN,PD,PY,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Ceramic capacitor mounting structure
Montagestruktur für einen keramischen Kondensator
Structure de montage pour un condensateur ceramique
PATENT (CC, No, Kind, Date): EP 978854 A2 000209 (Basic)

...ABSTRACT A2

A ceramic capacitor mounting structure comprising a flat capacitor element, and two **electrodes** connected respectively between opposite surfaces of said capacitor element, and having extensions which extend outwards from the periphery of the capacitor element, being structured in such a manner that by virtue of the **electrode** extensions it is capable of being connected to and released from connectors which are connected to bus bars or similar elements.

CLAIMS 1. A ceramic capacitor mounting structure, comprising:

- a flat capacitor element;
- first and second **electrodes** connected to an opposite surface of said capacitor element respectively, and having extension member which extend outward from the periphery of said capacitor element respectively; and
- first and second connectors attachable to said extension member of said first and second **electrodes** respectively.

2. A ceramic capacitor mounting structure, comprising:

- a ceramic capacitor comprising:
 - a flat capacitor element;
 - a first and second **electrodes** connected respectively to opposite surfaces of said capacitor element; wherein said ceramic capacitor is located between direct-current terminals of an inveter designed to permit a two-level alternating-current output; and
- said direct-current terminals and said first and second **electrodes** being connected electrically and mechanically.

3. A ceramic capacitor mounting structure, comprising:

- a ceramic capacitor comprising:
 - a flat capacitor element;
 - a first and second **electrodes** connected respectively to opposite surfaces of said capacitor element; wherein two ceramic capacitors are respectively located between a neutral terminal and direct-current terminals of an inverter to permit a three-level alternating-current output; and
- said neutral terminal and said first and second **electrodes** being each connected electrically and mechanically.

4. A ceramic capacitor mounting structure, comprising:

- a flat capacitor element;
- a single **electrode** connected electrically to a surface of said capacitor element;
- an **electrode** body connected electrically to the other surface of said capacitor element; and
- a coolant passage structuring member fashioned integrally with said **electrode** body and **carrying** a coolant to facilitate the

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cooling of said **electrode** body.

5. A ceramic capacitor mounting structure, comprising:
 - a flat capacitor element;
 - a single **electrode** connected electrically to a surface of said capacitor element;
 - an **electrode** body connected electrically to the other surface of said capacitor element; and
 - a cooling fin fashioned integrally with said **electrode** body and serving to increase the radiation effect.

09/26/2002 09/939,457

71/TI,PN,PD,PY,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME, CIRCUIT
SUBSTRATE, AND ELECTRONIC DEVICE
HALBLEITERBAUELEMENT UND DESSEN HERSTELLUNGSVERFAHREN, BAUELEMENTSUBSTRAT,
UND ELEKTRONISCHES BAUELEMENT
DISPOSITIF A SEMI-**CONDUCTEURS** ET SON PROCEDE DE FABRICATION, SUBSTRAT
A CIRCUITS ET DISPOSITIF ELECTRONIQUE
PATENT (CC, No, Kind, Date): EP 996154 A1 000426 (Basic)
WO 9950906 991007

DISPOSITIF A SEMI-**CONDUCTEURS** ET SON PROCEDE DE FABRICATION, SUBSTRAT
A CIRCUITS ET DISPOSITIF ELECTRONIQUE

...ABSTRACT present invention relates to a semiconductor device, and method of manufacture thereof, a circuit board, and an electronic instrument in which cracks in the external **electrodes** can be prevented. The semiconductor device comprises an **insulating film** (14) in which penetrating holes (14a) are formed, a **semiconductor chip** (12) having **electrodes** (13), a wiring pattern (18) adhered by an adhesive (17) over a region including penetrating holes (14a) on one side of the **insulating film** (14) and electrically connected to the **electrodes** (13) of the **semiconductor chip** (12), and external **electrodes** (16) provided on the wiring pattern (18) through the penetrating holes (14a) and projecting from the surface opposite to the surface of the substrate on which the wiring pattern (18) is formed. Part of the adhesive (17) is drawn in to be interposed between the penetrating holes (14a) and external **electrodes** (16).

CLAIMS 1. A semiconductor device comprising:
a substrate in which penetrating holes are formed;
a **semiconductor chip** having **electrodes**;
a **conductive** member adhered on one side of said substrate by an adhesive material over a particular region of said one side including said penetrating holes, and electrically connected to said **electrodes** of said **semiconductor chip** on the side opposite to the surface of being adhered by said adhesive; and
external **electrodes** which are provided through said penetrating holes, electrically connected to said **conductive** member, and extending as far as outside of the other side of said substrate;

wherein a part of said adhesive material is interposed between internal wall surfaces forming said penetrating holes and said external **electrodes** within said penetrating holes.

2. The semiconductor device as defined in claim 1,

wherein a part of said adhesive material enters and exists within said penetrating holes.

3. A semiconductor device comprising:
a substrate in which penetrating holes are formed;
a **semiconductor chip** having **electrodes**;

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- a **conductive** member directly formed over a particular region including said penetrating holes on one side of said substrate, and electrically connected to said **electrodes** of said **semiconductor chip**; and
- external **electrodes** which are provided through said penetrating holes, electrically connected to said **conductive** member, and extending as far as outside of the other side of said substrate;
- conductive** particles dispersed in an adhesive.
22. The semiconductor device as defined in claim 1,
- wherein said **electrodes** of said **semiconductor chip** are electrically connected to said **conductive** member through wires.
23. The semiconductor device as defined in claim 3,
- wherein said **electrodes** of said **semiconductor chip** are electrically connected to said **conductive** member through wires.
24. The semiconductor device as defined in claim 6,
- wherein said **electrodes** of said **semiconductor chip** are electrically connected to said **conductive** member through wires.

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71/TI,PN,PD,PY,K/4 (Item 4 from file: 348)
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ELECTRIC CABLE
ELEKTRISCHES KABEL
CABLE ELECTRIQUE

PATENT (CC, No, Kind, Date): EP 1070368 A1 010124 (Basic)
EP 1070368 B1 020130
WO 9946832 990916

...CLAIMS B1

1. An electric cable for **carrying** current from a current source to a consumer which has at least one interrupt area bordered by terminal sections (7) of the cable (1), with...

...for interrupting the current flow being arranged in this interrupt area, characterized in that the component is a controllable semiconductor component (3), in particular a **semiconductor chip** whose contact surfaces (8, 9) which are effective in current flow are connected to the end faces of the terminal sections (7) of the cable ...

...1, 2 or 3, characterized in that the metallic housing and/or the surfaces of the terminal segments of the cable are at least partially **coated** with electric **insulation**.

5. The electric cable according to Claims 1, 2 or 3, characterized in that an electrically insulating washer is arranged between the metallic housing and...

10. The electric cable according to one of the preceding claims, characterized in that the semiconductor component (33) has a control **electrode** (34) whose effective contact surface is connected to an electric control unit by way of a contacting means (38, 39) arranged in the interrupt area...

...in that the contacting means is an optoelectronic receiver.

19. The electric cable according to one of the preceding claims, characterized in that the control **electrode** is arranged centrally with respect to the semiconductor surfaces which are effective in current flow.

20. The electric cable according to Claim 19, characterized in that the control **electrode** is circular.

21. The electric cable according to Claim 19, characterized in that the control **electrode** has a polygonal border.

...CLAIMS cable et dans laquelle est dispose un composant pour l'interruption du passage du courant, caracterise en ce que le composant est un composant semi-**conducteur** (3) controlable, en particulier une puce semi-**conductrice**, dont des surfaces de contact (8, 9) actives pour le passage du courant sont en liaison avec les extremités avant des parties de raccordement (7...

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71/TI,PN,PD,PY,K/5 (Item 5 from file: 348)
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CHIP CARD, PROCESS FOR MANUFACTURING A **CHIP** CARD AND
SEMICONDUCTOR CHIP FOR USE IN A CHIP CARD
CHIPKARTE, VERFAHREN ZUR HERSTELLUNG EINER CHIPKARTE UND HALBLEITERCHIP ZUR
VERWENDUNG IN EINER CHIPKARTE
CARTE A PUCE, PROCEDE DE FABRICATION D'UNE CARTE A PUCE, ET PUCE DE SEMI-
CONDUCTEUR UTILISABLE DANS UNE CARTE A PUCE
PATENT (CC, No, Kind, Date): EP 978093 A1 000209 (Basic)
EP 978093 B1 011017
WO 9807113 980219

CHIP CARD, PROCESS FOR MANUFACTURING A **CHIP** CARD AND
SEMICONDUCTOR CHIP FOR USE IN A CHIP CARD
CARTE A PUCE, PROCEDE DE FABRICATION D'UNE CARTE A PUCE, ET PUCE DE SEMI-
CONDUCTEUR UTILISABLE DANS UNE CARTE A PUCE

...CLAIMS B1

1. Smart card having a card body (1) and a plurality of contact areas which are fabricated from electrically **conductive** material and are electrically connected to contact terminals (11), which are assigned to an electronic circuit formed on the semiconductor substrate (10) of a **semiconductor chip** (4),

characterized in that

the contact areas (3) are fabricated in the form of a structured coating on a main surface of the **semiconductor chip** (4), the said main surface facing the electronic circuit, with the result that the contact areas (3) are completely supported by the semiconductor substrate (10) of the **semiconductor chip** (4), and the **semiconductor chip** (4) fabricated together with the contact areas (3) is inserted and fixed in a receptacle opening (2) in the card body (1) of the smart...

- ...3) extend essentially flush with the outer face (7) of the card body (1).

2. Smart card according to Claim 1, characterized in that the **semiconductor chip** (4) **carrying** the contact areas (3) on its main surface is fixed permanently within the receptacle opening (2) in the card body (1) by means of an...

...in particular preferably about 100 (mu)m or less.

4. Smart card according to one of Claims 1 to 3, characterized in that a thin **insulation layer** (9) is applied on the main surface of the semiconductor substrate (10) **carrying** the **electronic** circuit, on which **insulation layer** the contact areas (3) are deposited in the form of a structured coating.
5. **Semiconductor chip** having contact terminals (11), which are assigned to an electrical circuit formed on the semiconductor substrate (10) of the **semiconductor chip** (4),

characterized in that

contact areas (3) electrically connected to the contact terminals (11) are fabricated in the form of a structured coating on a main surface of the **semiconductor chip** (4), the said main surface facing the circuit, with the result that the contact areas (3) are completely supported by the semiconductor substrate (10) of the **semiconductor chip** (4).

6. **Semiconductor chip** according to Claim 5, characterized in that a thin **insulation layer** (9) is applied on the main surface of the semiconductor substrate (10) **carrying** the **electronic circuit**, on which **insulation layer** the contact areas (3) are deposited in the form of a structured coating.
7. **Semiconductor chip** according to one of Claims 5 to 6, characterized in that the thickness of the semiconductor substrate (10), which is preferably composed of silicon, for...

...flexibility, is distinctly less than 200 (μ m), preferably about 150 (μ m) or less, in particular preferably about 100 (μ m) or less.

8. **Semiconductor chip** according to Claim 7, characterized in that the thickness of the semiconductor substrate (10), which is preferably composed of silicon, is about 50 (μ m) to about 100 (μ m).
9. **Semiconductor chip** according to one of Claims 5 to 8, characterized in that the total thickness of the electrically **conductive coating** (12) for the contact areas (3) is about 30 (μ m) to about 50 (μ m).
10. **Semiconductor chip** according to one of Claims 5 to 9, characterized in that the electrically **conductive coating** (12) for the contact areas (3) comprises a plurality of electrically **conductive layers**.

...CLAIMS B1

1. Carte a puce comprenant un corps (1) de carte et plusieurs surfaces de contact en un materiau **conducteur** de l'electricite, qui sont reliees electriquement a des homes (11) de contact, qui sont associees a un circuit electronique constitue d'une puce (4) a semi-**conducteur** sur le substrat (10) semi-**conducteur**, caracterisee en que les surfaces (3) de contact sont fabriquees sous la forme d'un revetement structure sur une surface principale de la puce (4) a semi-**conducteur** qui est tournee vers le circuit electronique, de facon que les surfaces (3) de contact soient soutenues entierement par le substrat (10) semi-**conducteur** de la puce (4) a semi-**conducteur**, et la puce (4) a semi-**conducteur** fabriquee en meme temps que les surfaces (3) de contact est inseree et fixee dans une ouverture (2) de reception du corps (1) de la...

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71/TI,PN,PD,PY,K/6 (Item 6 from file: 348)
DIALOG(R) File 348:(c) 2002 European Patent Office. All rts. reserv.

Interconnection process of stacked semi-**conductors** chips and devices
Verfahren, um gestapelte Halbleiterchips zusammenzuschalten und Bauelement
Procede d'interconnexion de pastilles semi-conductrices en trois
dimensions, et composant en resultant

PATENT (CC, No, Kind, Date): EP 638933 A1 950215 (Basic)
EP 638933 B1 990929

Interconnection process of stacked semi-**conductors** chips and devices

...ABSTRACT Translated)

According to the method of the invention, wafers (P) each formed of one or more **semiconductor chips** are equipped with **conductors** (F), wires for example, connected to the leads (PC))) of the chips and turned towards the side faces of the stack, then the chips are...

CLAIMS 1. Method for interconnecting wafers in three dimensions, the wafers comprising one or more **semiconductor chips**, the **chips** comprising pads for their interconnection, the process being characterized by the fact that it comprises the following steps in succession:

* connecting (11) leads (F, 36...

...characterized by the fact that, during the first step (11), each of the wafers (P) is arranged inside a frame (21) of electrically insulating material, **carrying conducting** depositions (22); that the leads (F) are connected between the pads (Pc))) and the **conducting** depositions, and that, during the fourth step (14), the lateral faces of the stack are treated so as to eliminate the frame.

3. Method according...

...the fact that, during the first step (11), each of the wafers (P) is arranged on a plate (23) of electrically insulating material, the plate **carrying conducting** depositions (24), and chat the leads (F) are connected between the pads (Pc))) and the **conducting** depositions.

4. Method according to Claim 1, characterized by the fact that, during the first step, each of the wafers (P) is arranged inside a frame (26) of electrically insulating material, the frame **carrying conducting** strips (27) extending (F) beyond the frame so as to come above the pads (Pc))) and being connected to the latter, and that, during the...

...according to one of the preceding claims, characterized by the fact that it further comprises a step (17) of coating the stack with an electrically **insulating layer** of a mineral material.

11. Component comprising interconnected wafers, the wafers comprising one or more **semiconductor chips**, the **chips** comprising

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71/TI,PN,PD,PY,K/7 (Item 7 from file: 348)
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Improved multi-layer packaging
Verbesserte Mehrschichtverpackung
Empaquetage multi-couche ameliore
PATENT (CC, No, Kind, Date): EP 617466 A2 940928 (Basic)
EP 617466 A3 941130
EP 617466 B1 980826

ance variations...

CLAIMS 1. A multi-layered package including a plurality of interleaved **layers** of **conductive** material and dielectric material surrounding a die-attach area of predetermined size, an array of external connectors (110) on one side of the package and...

...a plurality of via columns (150) electrically connecting each external connector of said array of external connectors to a predetermined horizontal path on a selected **layer** of **conductive** material, characterized in that

a **layer** of **conductive** material designed for **carrying** active signals (402) is sandwiched between an upper **layer** of **conductive** material (403) designed for **carrying** a first shield signal and a lower **layer** of **conductive** material (401) designed for **carrying** a second shield signal, wherein the first and second shield signals have opposite polarities.

2. A multi-layered package as recited in claim 1, further characterized in that a signal path (420) on the **layer** of **conductive** material **carrying** active signals (402) is co-planary shielded by a first shield path (430) disposed on a first side and a second shield path (440) on a second side, wherein the first shield path (430) connects to the lower **layer** of **conductive** material (401) through a via column (400) and the second shield path (440) connects to the upper **layer** of **conductive** material (403) through a via column (410).

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71/TI,PN,PD,PY,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor laser array
Vielfachhalbleiterlaser

Dispositif laser multiple a semi-conducteur
PATENT (CC, No, Kind, Date): EP 590232 A1 940406 (Basic)
EP 590232 B1 970806

Dispositif laser multiple a semi-conducteur

...ABSTRACT A1

A semiconductor laser device includes a **semiconductor** laser array **chip** (3) including a plurality of active regions (4a,4b,4c), each region being driven independently, and a heat sink (2) comprising a plurality of **layers** comprising an **insulating** material having relatively high thermal conductivity (2a) and a plurality of **layers** comprising an **insulating** material having relatively low thermal conductivity (2b), which are alternately laminated in the array direction of the active regions (4a,4b,4c). The **semiconductor** laser array **chip** (3) is disposed on the heat sink (2) so that at least one of the low thermal conductivity layers (2b) of the heat sink (2...

...CLAIMS A1

1. A semiconductor laser device comprising a **semiconductor** laser array **chip** (3) including a plurality of stripe-shaped active regions (4a,4b,4c), each active region being driven independently, and a heat sink (2) on which said **semiconductor** laser array **chip** (3) is disposed, wherein:
said heat sink (2) comprising a plurality of **layers** comprising an **insulating** material having relatively high thermal conductivity (2a) and a plurality of **layers** comprising an **insulating** material having relatively low thermal conductivity (2b), which are alternately laminated in the array direction of said active regions (4a,4b,4c); and
said **semiconductor** laser array **chip** (3) being disposed on said heat sink (2) so that at least one of said layers having relatively low thermal conductivity (2b) is present beneath each region between adjacent active regions.
2. A semiconductor laser device comprising a **semiconductor** laser array **chip** (3) including a plurality of stripe-shaped active regions (4), each region being independently driven, and a heat sink (2) on which said **semiconductor** laser array **chip** (3) is disposed, wherein:
said heat sink (2) comprising a plurality of layers comprising a material having relatively high thermal conductivity (23) and a plurality...

...so that a thermal expansion coefficient of the whole heat sink (2) is equivalent to a thermal expansion coefficient of a principal material of said **semiconductor** laser array **chip** (3); and
said **semiconductor** laser array **chip** (3) being

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disposed on said heat sink so that at least one of said relatively low thermal conductivity layers (24) is present beneath each region between adjacent active regions.

3. A semiconductor laser device comprising a **semiconductor** laser array **chip** (3) including a plurality of stripe-shaped active regions (4a,4b,4c,4d), each region being driven independently, and a heat sink (2) on which said **semiconductor** laser array **chip** (3) is disposed, wherein:

said heat sink (2) including a plurality of stripe grooves (8) having a prescribed depth from the surface of said heat sink (2) and periodically disposed in the array direction of said active regions (4a,4b,4c,4d);

to the rear surface thereof.

5. A semiconductor laser device comprising a **semiconductor** laser array **chip** (3) including a plurality of stripe-shaped active regions (4a,4b,4c), each region being driven independently, and a heat sink (26) on which said **semiconductor** laser array **chip** (3) is disposed, wherein:

said heat sink (26) comprising a polycrystalline layer including columnar or fiber grains; and

said **semiconductor** laser array **chip** (3) being disposed on a surface of said heat sink (26), which surface is perpendicular to the length of said grain.

6. The semiconductor laser device of one of claims 1 to 5 wherein a plurality of independent **semiconductor** laser **chips**, each **chip** including a stripe-shaped active region, are employed as said **semiconductor** laser array **chip**.

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71/TI,PN,PD,PY,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Process for making a contact to a semiconductor device
Verfahren zum Herstellen eines Kontakts auf einem Halbleiterbauelement
Procede de prise de contact sur un composant semiconducteur
PATENT (CC, No, Kind, Date): EP 514297 A2 921119 (Basic)
EP 514297 A3 940601
EP 514297 B1 961218

...ABSTRACT Translated)

The present invention relates to a process for making a contact on one face of a **semiconductor chip** comprising a diffused region (3) delimited by an **insulating layer** forming a mask (4). This process comprises the following steps:

a) forming a layer (11) of doped polycrystalline silicon and delimiting this layer so that...

.CLAIMS B1

1. A method of forming a metal contact on a surface of a **semiconductor chip** comprising a diffusion region (3) delineated by an isolating layer forming a mask (4), said chip being part of a semiconductor wafer, comprising the steps...

...diffused region and overlaps the internal peripheral surfaces of said mask;

- (b) immersing said wafer in a metal-plating electroless bath to deposit a metallization **layer** (12, 13) on **conductive** surfaces of said wafer including said polysilicon layer; and
- (c) after each metal-plating, immersing said wafer in a selective etching bath for partially etching away said mask.
2. The method according to claim 1, wherein step (b) comprises immersing said **semiconductor chip** in at least one nickel-plating electroless bath followed by immersing in a gold-plating electroless bath.
3. The method according to claim 2, wherein...